S812

Quick Reference Manual

Revision: 0.6

Release date: 9/4/2014

Amlogic, Inc.

REVISION HISTORY

Revision Number	Revision Date	Changes
0.1	2014/1/7	Initial draft
0.2	2014/2/20	Correct SDIO number and GPIOAO_0~6 default status
0.3	2014/4/21	Update operation condition and power on sequence
0.4	2014/5/12	Add thermal operating spec and notes on USB VBUS voltage; Correct L2 cache size
0.5	2014/7/15	Correct BOOT_0 default PU/PD; Update power on sequence
0.6	2014/9/2	Update operating conditions

CONTACT INFORMATION

Amlogic, Inc.
2518 Mission College Blvd, Ste 120
Santa Clara, CA 95054
U.S.A.
www.amlogic.com

Contents

1. General Description

S812 is an advanced application processor designed for Set Top Box (STB) and high-end media player applications. It integrates a powerful CPU/GPU subsystem, and a secured 4K video CODEC engine with all major peripherals to form the ultimate low power multimedia AP.

The main system CPU is a quad core ARM Cortex-A9r4 CPU with 32KB L1 instruction and 32KB data cache for each core and a large 1MB L2 unified cache to improve system performance. In addition, the Cortex-A9 CPU includes the NEON SIMD co-processor to improve software media processing capability. The quad core ARM Cortex-A9 CPU can run up to 2GHz and has a wide bus connecting to the memory sub-system.

The graphic subsystem consists of eight graphic engines and a flexible video/graphic output pipeline. The eight core ARM Mali-450 GPU including dual geometry processors (GP) and six pixel processors (PP) handles all the OpenGL ES 1.1/2.0 and OpenVG graphics programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. The video output pipeline can perform advanced image correction and enhancements. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks.

Four additional processors offload the Cortex-A9 CPUs by handling all audio and video CODEC processing – the MediaCPU and tri-core Amlogic Video Engine (AVE) including dedicated hardware video decoders and encoders. The MediaCPU is audio optimized and handles all audio decoding tasks. The scalable tri-core AVE is capable of decoding 4K2K resolution video with complete Trusted Video Path (TVP) for secure applications and supports full formats including MVC, MPEG-1/2/4, VC-1/WMV, AVS, RealVideo, MJPEG streams, H.264, H.265 and also JPEG pictures with no size limitation. The independent encoder is able to encode in JPEG and H.264 up to 1080p at 30fps.

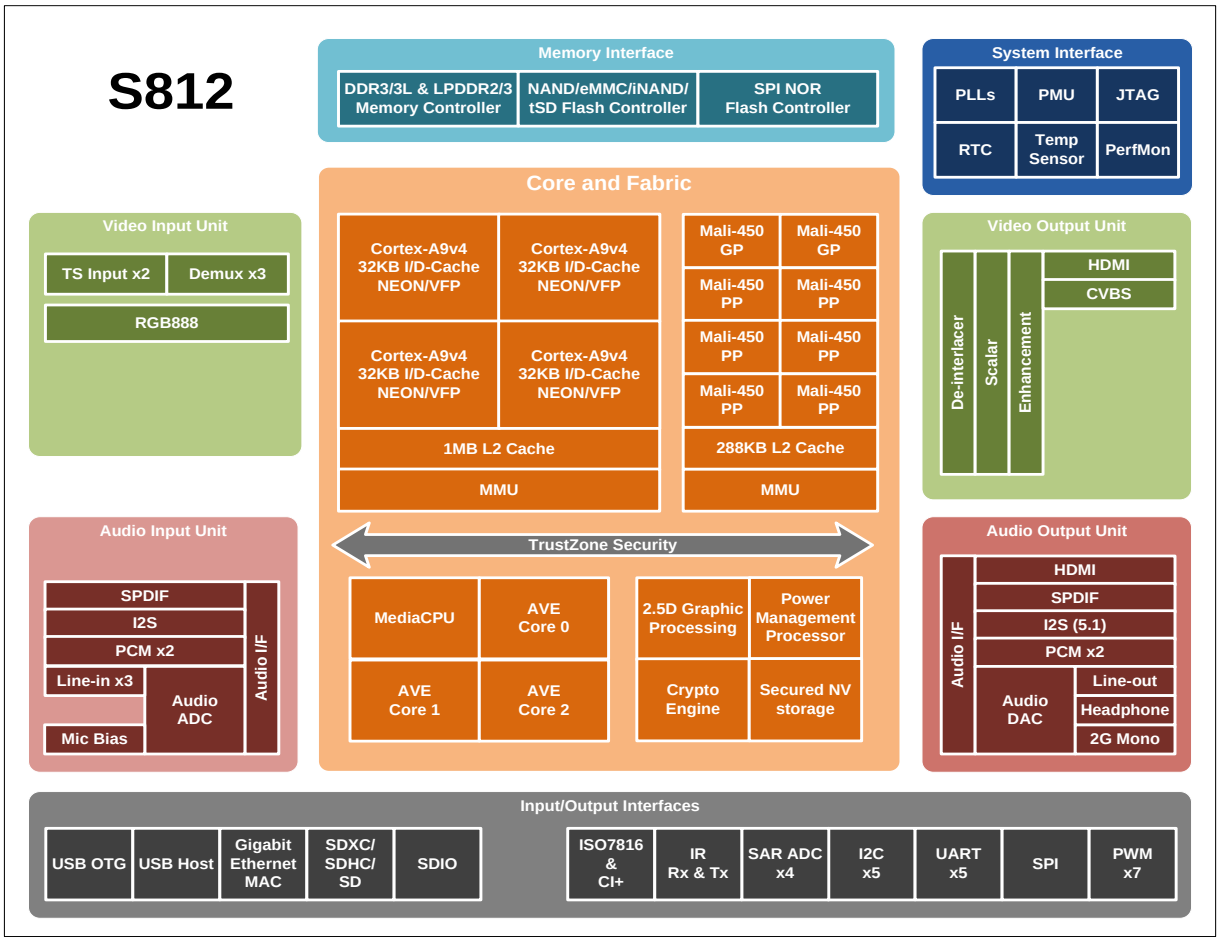
S812 integrates all standard audio/video input/output interfaces including an HDMI1.4b transmitter with 3D support, 4K UHD output, CEC and HDCP, a CVBS output, a complete audio CODEC with headphone PA and microphone bias, I2S and SPDIF digital audio input/output interfaces and a PCM audio interface.

S812 integrates a set of functional blocks for digital TV broadcasting streams. The built-in three demux can process the TV streams from two transport stream input interfaces, which can connect to tuner/demodulator and CI+ module. An ISO7816 smart card interface and a crypto-processor built in to help handling encrypted traffic and media streams.

The processor has rich advanced network and peripheral interfaces, including a Gigabit Ethernet MAC with RGMII interface, dual USB 2.0 high-speed ports (one OTG and one HOST), three SDIOs with multi-standard memory card controller, five UART interfaces, five I2C interfaces, one high-speed SPI interface and seven PWMs.

Standard development environment utilizing GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

2. Features Summary



CPU Sub-system

- Quad core ARM Cortex-A9r4 CPU up to 2GHz (DVFS) and 20,000DMIPS
- ARMv7 instruction set, multi-issue superscalar, out-of-order architecture with dynamic branch prediction
- 32KB instruction cache and 32KB data cache
- 1MB Unified L2 cache
- Advanced NEON and VFP co-processor
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

3D Graphics Processing Unit

- Eight core ARM Mali-450 GPU up to 600MHz+ (DVFS)
- Dual Geometry Processors with 32KB L2 cache
- Six Pixel Processors with 2x 128KB L2 caches
- Concurrent multi-core processing
- 3600Mpix/sec and 132Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support

2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter
- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

Crypto Engine

- Supports AES block cipher with 128/192/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- Supports DES/3DES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- Built-in LSFR Random number generator

Video/Picture CODEC

- Tri-cores Amlogic Video Engine (AVE) based on scalable multi-core architecture with dedicated hardware decoders an encoders
- Hardware based trusted video path (TVP)
- Supports multiple “secured” video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
    - H.265 HEVC MP@L5.0 up to 4Kx2K@30fps
    - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
    - H.264 MVC up to 1080P@60fps
    - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
    - WMV/VC-1 SP/MP/AP up to 1080P@60fps
    - AVS JiZhun Profile up to 1080P@60fps
    - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
    - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
    - RealVideo 8/9/10 up to 1080P
    - WebM up to VGA
    - Multiple language and multiple format sub-title video support
    - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
    - Supports JPEG thumbnail, scaling, rotation and transition effects
    - Supports *.mkv,*.wmv,*.mpg, *.mpeg, *.dat, *.avi, *.mov, *.iso, *.mp4, *.rm and *.jpg file formats
- Video/Picture Encoding
    - Independent JPEG and H.264 encoder with configurable performance/bit-rate
    - JPEG image encoding
    - H.264 video encoding up to 1080P@30fps

Video Post-Processing Engine

- Motion adaptive 3D noise reduction filter
- Advanced motion adaptive edge enhancing de-interlacing engine
- 3:2 pull-down support
- Programmable poly-phase scalar for both horizontal and vertical dimension for zoom and windowing
- Programmable color management filter (to enhance blue, green, red, face and other colors)
- Dynamic Non-Linear Luma filter
- Programmable color matrix pipeline
- Video mixer: 2 video planes and 2 graphics planes per video output

Video Output

- Built-in HDMI 1.4b transmitter including both controller and PHY with CEC and HDCP, 4Kx2K@30 max resolution output
- CVBS 480i/576i standard definition output
- Supports all standard SD/HD/UHD video output formats: 480i/p, 576i/p, 720p ,1080i/p and 4Kx2K
- Supports dual video output with combination of CVBS+HDMI
- Supports 3D HDMI display

Audio CODEC and Input/Output

- Low power MediaCPU with DSP audio processing
- Supports MP3, AAC, WMA, RM, FLAC, Ogg and programmable with 5.1 down-mixing
- Internal audio CODEC supporting 3 channels stereo input, 1 channel stereo HP/SPK output and 1 channel 2G mono output
- I2S audio interface supporting 6-channel(5.1) out and 2-channel in
- Built-in SPDIF/IEC958 and PCM serial digital audio input/output
- Supports concurrent dual audio stereo channel output with combination of analog+PCM or I2S+PCM

Memory and Storage Interface

- Dual-channel 32-bit SDRAM memory interface running up to DDR1600 and supporting asymmetric mode
- Supports up to 4GB DDR3, DDR3L, LPDDR2 and LPDDR3 memory
- TrustZone protected DRAM memory region and internal SRAM
- Supports SLC/MLC/TLC NAND Flash with 60-bit ECC, compatible to ONFI 2.1 and Toggle 2.0 mode
- SDSC/SDHC/SDXC card and SDIO interface with 1-bit and 4-bit data bus width supporting spec version 2.x/3.x/4.x DS/HS modes up to UHS-I SDR50
- eMMC and MMC card interface with 1/4/8-bit data bus width supporting spec version 4.4x/4.5x HS200 (up to 100MHz clock), compatible with standard iNAND interface
- Supports serial 1, 2 or 4-bit NOR Flash via SPI interface
- Built-in 4k bits One-Time-Programming ROM for key storage

Network

- Integrated IEEE 802.3 Gigabit Ethernet controller with RGMII interface
- Optional 50MHz clock output to Ethernet PHY
- WiFi/IEEE802.11 & Bluetooth supporting via SDIO/USB/UART/PCM

Digital Television Interface

- Two transport stream(TS) input interfaces with three built-in demux processor for connecting to external digital TV tuner/demodulator and one output TS interface
- Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
- Integrated CI+ ports and ISO 7816 smart card controller

Integrated I/O Controllers and Interfaces

- Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
- 5 UART, 5 I2C and SPI interface with 3 slave selects
- Seven PWMs
- Programmable IR remote input/output controllers
- Built-in 10bit SAR ADC with 4 input channels
- A set of General Purpose IO interfaces with built-in pull up and pull down

System, Peripherals and Misc. Interfaces

- Integrated general purpose timers, counters, DMA controllers
- Integrated RTC with battery backup option
- 24 MHz and 32 KHz crystal oscillator input
- Embedded debug interface using ICE/JTAG

Power Management

- Multiple external power domains controlled by PMIC
- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs for DVFS operation
- Multi-voltage I/O design for 1.8V and 3.3V
- Power management auxiliary processor in dedicated always-on (AO) power domain to communicate with external PMIC

Security

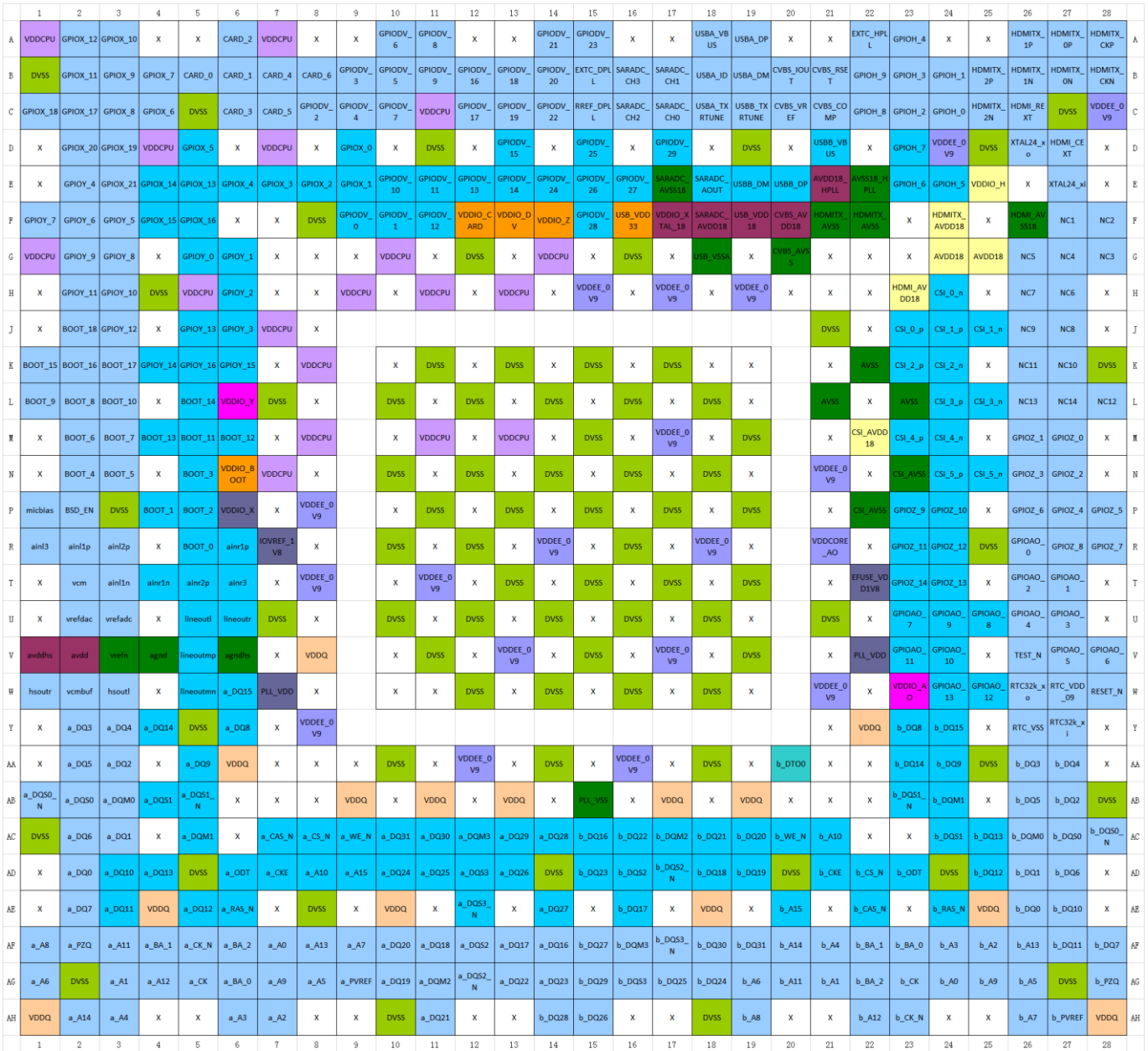
- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, OTP, internal control buses and storage
- Protected memory regions and scrambled memory data interface
- Trusted Video Path and Secured (needs SecureOS software)

Package

- LFBGA, 19x19mm, 531-ball, 0.65 ball pitch, RoHS compliant

3. Pin Out Specification

3.1 Pin-Out Diagram (top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	VDDCPU	GPIOX_12	GPIOX_10	X	X	CARD_2	VDDCPU	X	X	GPIODV_6	GPIODV_8	X	X	GPIODV_21	GPIODV_23	X	X	USBA_VBUS	USBA_DP	X	X	EXTC_HPLL	GPIOH_4	X	X	HDMITX_1P	HDMITX_0P	HDMITX_CKP	A
B	DVSS	GPIOX_11	GPIOX_9	GPIOX_7	CARD_0	CARD_1	CARD_4	CARD_6	GPIODV_3	GPIODV_5	GPIODV_9	GPIODV_16	GPIODV_18	GPIODV_20	EXTC_DPLL	SARADC_CH3	SARADC_CH1	USBA_ID	USBA_DM	CVBS_IOUT	CVBS_RSET	GPIOH_9	GPIOH_3	GPIOH_1	HDMITX_2P	HDMITX_1N	HDMITX_0N	HDMITX_CKN	B
C	GPIOX_18	GPIOX_17	GPIOX_8	GPIOX_6	DVSS	CARD_3	CARD_5	GPIODV_2	GPIODV_4	GPIODV_7	VDDCPU	GPIODV_17	GPIODV_19	GPIODV_22	RREF_DPLL	SARADC_CH2	SARADC_CH0	USBA_TXRTUNE	USBB_TXRTUNE	CVBS_VREF	CVBS_COMP	GPIOH_8	GPIOH_2	GPIOH_0	HDMITX_2N	HDMI_REXT	DVSS	VDDEE_0V9	C
D	X	GPIOX_20	GPIOX_19	VDDCPU	GPIOX_5	X	VDDCPU	X	GPIOX_0	X	DVSS	X	GPIODV_15	X	GPIODV_25	X	GPIODV_29	X	DVSS	X	USBB_VBUS	X	GPIOH_7	VDDEE_0V9	DVSS	XTAL24_xo	HDMI_CEXT	X	D
E	X	GPIOY_4	GPIOX_21	GPIOX_14	GPIOX_13	GPIOX_4	GPIOX_3	GPIOX_2	GPIOX_1	GPIODV_10	GPIODV_11	GPIODV_13	GPIODV_14	GPIODV_24	GPIODV_26	GPIODV_27	SARADC_AVSS18	SARADC_AOUT	USBB_DM	USBB_DP	AVDD18_HPLL	AVSS18_HPLL	GPIOH_6	GPIOH_5	VDDIO_H	X	XTAL24_xi	X	E
F	GPIOY_7	GPIOY_6	GPIOY_5	GPIOX_15	GPIOX_16	X	X	DVSS	GPIODV_0	GPIODV_1	GPIODV_12	VDDIO_CARD	VDDIO_DV	VDDIO_Z	GPIODV_28	USB_VDD33	VDDIO_XTAL_18	SARADC_AVDD18	USB_VDD18	CVBS_AVDD18	HDMITX_AVSS	HDMITX_AVSS	X	HDMITX_AVDD18	X	HDMI_AVSS18	NC1	NC2	F
G	VDDCPU	GPIOY_9	GPIOY_8	X	GPIOY_0	GPIOY_1	X	X	X	VDDCPU	X	DVSS	X	VDDCPU	X	DVSS	X	USB_VSSA	X	CVBS_AVSS	X	X	X	AVDD18	AVDD18	NC5	NC4	NC3	G
H	X	GPIOY_11	GPIOY_10	DVSS	VDDCPU	GPIOY_2	X	X	VDDCPU	X	VDDCPU	X	VDDCPU	X	VDDEE_0V9	X	VDDEE_0V9	X	VDDEE_0V9	X	X	X	HDMI_AVDD18	CSI_0_n	X	NC7	NC6	X	H
J	X	BOOT_18	GPIOY_12	X	GPIOY_13	GPIOY_3	VDDCPU	X													DVSS	X	CSI_0_p	CSI_1_p	CSI_1_n	NC9	NC8	X	J
K	BOOT_15	BOOT_16	BOOT_17	GPIOY_14	GPIOY_16	GPIOY_15	X	VDDCPU		X	DVSS	X	DVSS	X	DVSS	X	DVSS	X	X		X	AVSS	CSI_2_p	CSI_2_n	X	NC11	NC10	DVSS	K
L	BOOT_9	BOOT_8	BOOT_10	X	BOOT_14	VDDIO_Y	DVSS	X		DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		AVSS	X	AVSS	CSI_3_p	CSI_3_n	NC13	NC14	NC12	L
M	X	BOOT_6	BOOT_7	BOOT_13	BOOT_11	BOOT_12	X	VDDCPU		X	VDDCPU	X	VDDCPU	X	DVSS	X	VDDEE_0V9	X	DVSS		X	CSI_AVDD18	CSI_4_p	CSI_4_n	X	GPIOZ_1	GPIOZ_0	X	M
N	X	BOOT_4	BOOT_5	X	BOOT_3	VDDIO_BOOT	VDDCPU	X		DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		VDDEE_0V9	X	CSI_AVSS	CSI_5_p	CSI_5_n	GPIOZ_3	GPIOZ_2	X	N
P	micbias	BSD_EN	DVSS	BOOT_1	BOOT_2	VDDIO_X	X	VDDEE_0V9		X	DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS		X	CSI_AVSS	GPIOZ_9	GPIOZ_10	X	GPIOZ_6	GPIOZ_4	GPIOZ_5	P
R	ainl3	ainl1p	ainl2p	X	BOOT_0	ainr1p	IOVREF_1V8	X		DVSS	X	DVSS	X	VDDEE_0V9	X	DVSS	X	VDDEE_0V9	X		VDDCORE_AO	X	GPIOZ_11	GPIOZ_12	DVSS	GPIOAO_0	GPIOZ_8	GPIOZ_7	R
T	X	vcm	ainl1n	ainr1n	ainr2p	ainr3	X	VDDEE_0V9		X	VDDEE_0V9	X	DVSS	X	DVSS	X	DVSS	X	DVSS		X	EFUSE_VDD1V8	GPIOZ_14	GPIOZ_13	X	GPIOAO_2	GPIOAO_1	X	T
U	X	vrefdac	vrefadc	X	lineoutl	lineoutr	DVSS	X		DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		DVSS	X	GPIOAO_7	GPIOAO_9	GPIOAO_8	GPIOAO_4	GPIOAO_3	X	U
V	avddhs	avdd	vrefn	agnd	lineoutmp	agndhs	X	VDDQ		X	DVSS	X	VDDEE_0V9	X	DVSS	X	VDDEE_0V9	X	DVSS		X	PLL_VDD	GPIOAO_11	GPIOAO_10	X	TEST_N	GPIOAO_5	GPIOAO_6	V
W	hsoutr	vcmbuf	hsoutl	X	lineoutmn	a_DQ15	PLL_VDD	X		X	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		VDDEE_0V9	X	VDDIO_AO	GPIOAO_13	GPIOAO_12	RTC32k_xo	RTC_VDD_09	RESET_N	W
Y	X	a_DQ3	a_DQ4	a_DQ14	DVSS	a_DQ8	X	VDDEE_0V9													X	VDDQ	b_DQ8	b_DQ15	X	RTC_VSS	RTC32k_xi	X	Y
AA	X	a_DQ5	a_DQ2	X	a_DQ9	VDDQ	X	X	X	DVSS	X	VDDEE_0V9	X	DVSS	X	VDDEE_0V9	X	DVSS	X	b_DTO0	X	X	b_DQ14	b_DQ9	DVSS	b_DQ3	b_DQ4	X	AA
AB	a_DQS0_N	a_DQS0	a_DQM0	a_DQS1	a_DQS1_N	X	X	X	VDDQ	X	VDDQ	X	VDDQ	X	PLL_VSS	X	VDDQ	X	VDDQ	X	X	X	b_DQS1_N	b_DQM1	X	b_DQ5	b_DQ2	DVSS	AB
AC	DVSS	a_DQ6	a_DQ1	X	a_DQM1	X	a_CAS_N	a_CS_N	a_WE_N	a_DQ31	a_DQ30	a_DQM3	a_DQ29	a_DQ28	b_DQ16	b_DQ22	b_DQM2	b_DQ21	b_DQ20	b_WE_N	b_A10	X	X	b_DQS1	b_DQ13	b_DQM0	b_DQS0	b_DQS0_N	AC
AD	X	a_DQ0	a_DQ10	a_DQ13	DVSS	a_ODT	a_CKE	a_A10	a_A15	a_DQ24	a_DQ25	a_DQS3	a_DQ26	DVSS	b_DQ23	b_DQS2	b_DQS2_N	b_DQ18	b_DQ19	DVSS	b_CKE	b_CS_N	b_ODT	DVSS	b_DQ12	b_DQ1	b_DQ6	X	AD
AE	X	a_DQ7	a_DQ11	VDDQ	a_DQ12	a_RAS_N	X	DVSS	X	VDDQ	X	a_DQS3_N	X	a_DQ27	X	b_DQ17	X	VDDQ	X	b_A15	X	b_CAS_N	X	b_RAS_N	VDDQ	b_DQ0	b_DQ10	X	AE
AF	a_A8	a_PZQ	a_A11	a_BA_1	a_CK_N	a_BA_2	a_A0	a_A13	a_A7	a_DQ20	a_DQ18	a_DQS2	a_DQ17	a_DQ16	b_DQ27	b_DQM3	b_DQS3_N	b_DQ30	b_DQ31	b_A14	b_A4	b_BA_1	b_BA_0	b_A3	b_A2	b_A13	b_DQ11	b_DQ7	AF
AG	a_A6	DVSS	a_A1	a_A12	a_CK	a_BA_0	a_A9	a_A5	a_PVREF	a_DQ19	a_DQM2	a_DQS2_N	a_DQ22	a_DQ23	b_DQ29	b_DQS3	b_DQ25	b_DQ24	b_A6	b_A11	b_A1	b_BA_2	b_CK	b_A0	b_A9	b_A5	DVSS	b_PZQ	AG
AH	VDDQ	a_A14	a_A4	X	X	a_A3	a_A2	X	X	DVSS	a_DQ21	X	X	b_DQ28	b_DQ26	X	X	DVSS	b_A8	X	X	b_A12	b_CK_N	X	X	b_A7	b_PVREF	VDDQ	AH
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	