S802

Quick Reference Manual

Revision: 0.5

Release date: 9/4/2014

Amlogic, Inc.

REVISION HISTORY

Revision Number	Revision Date	Changes
0.1	2013/9/29	Initial draft
0.2	2014/2/28	Correct SDIO number and spec, GPIOAO_0~6 default status
0.3	2014/4/21	Update operation condition and power on sequence
0.4	2014/5/12	Add thermal operating spec and notes on USB VBUS voltage
0.5	2014/9/2	Update operating conditions

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Contents

1. General Description

S802 is an advanced application processor designed for Set Top Box (STB) and high-end media player applications. It integrates a powerful CPU/GPU subsystem, and a secured 4K video CODEC engine with all major peripherals to form the ultimate low power multimedia AP.

The main system CPU is a quad core ARM Cortex-A9r4 CPU with 32KB L1 instruction and 32KB data cache for each core and a large 1MB L2 unified cache to improve system performance. In addition, the Cortex-A9 CPU includes the NEON SIMD co-processor to improve software media processing capability. The quad core ARM Cortex-A9 CPU can run up to 2GHz and has a wide bus connecting to the memory sub-system.

The graphic subsystem consists of eight graphic engines and a flexible video/graphic output pipeline. The eight core ARM Mali-450 GPU including dual geometry processors (GP) and six pixel processors (PP) handles all the OpenGL ES 1.1/2.0 and OpenVG graphics programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. The video output pipeline can perform advanced image correction and enhancements. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks.

Four additional processors offload the Cortex-A9 CPUs by handling all audio and video CODEC processing – the MediaCPU and tri-core Amlogic Video Engine (AVE) including dedicated hardware video decoders and encoders. The MediaCPU is audio optimized and handles all audio decoding tasks. The scalable tri-core AVE is capable of decoding 4K2K resolution video with complete Trusted Video Path (TVP) for secure applications and supports full formats including MVC, MPEG-1/2/4, VC-1/WMV, AVS, RealVideo, MJPEG streams, H.264, H.265 and also JPEG pictures with no size limitation. The independent encoder is able to encode in JPEG and H.264 up to 1080p at 30fps.

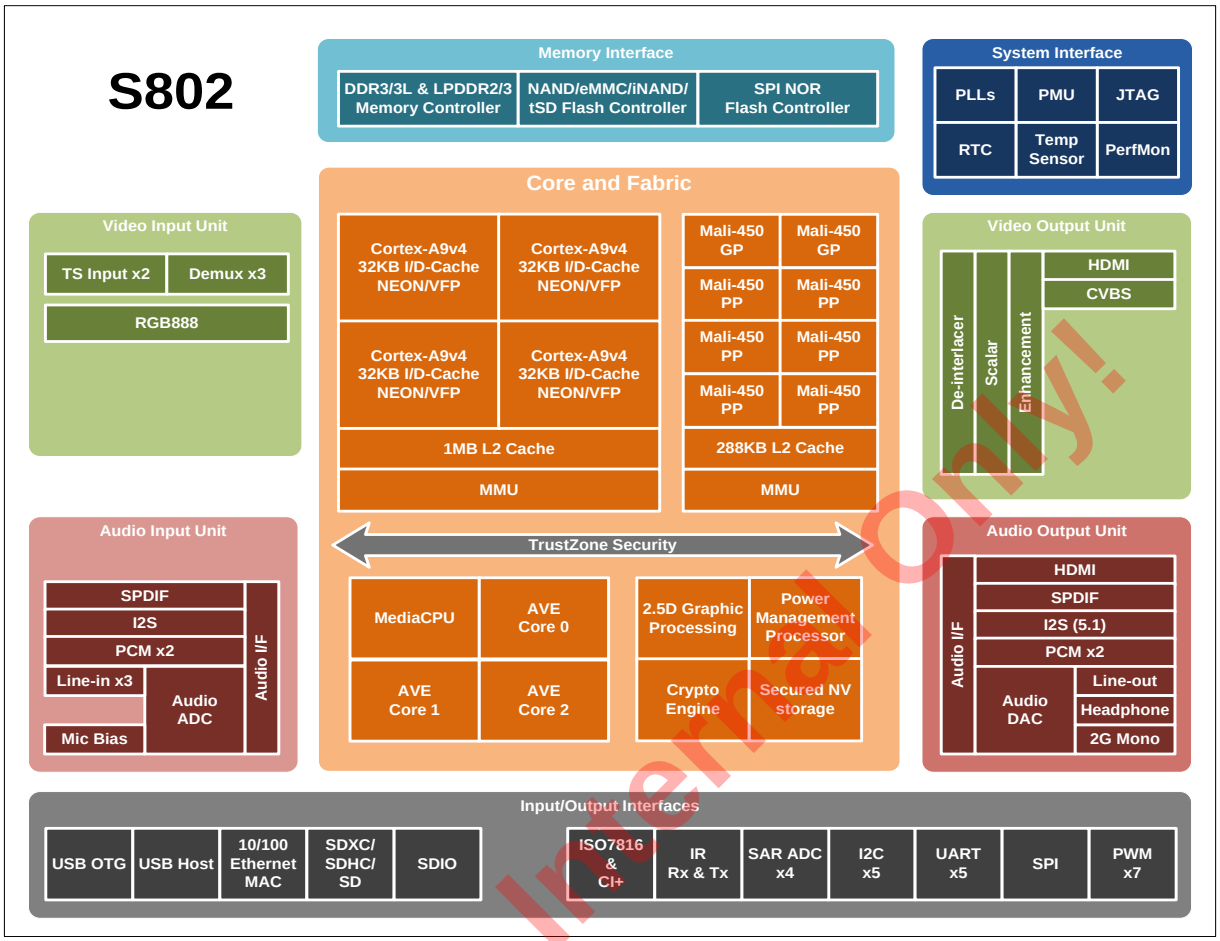
S802 integrates all standard audio/video input/output interfaces including an HDMI1.4b transmitter with 3D support, 4K UHD output, CEC and HDCP, a CVBS output, a complete audio CODEC with headphone PA and microphone bias, I2S and SPDIF digital audio input/output interfaces and a PCM audio interface.

S802 integrates a set of functional blocks for digital TV broadcasting streams. The built-in three demux can process the TV streams from two transport stream input interfaces, which can connect to tuner/demodulator and CI+ module. An ISO7816 smart card interface and a crypto-processor built in to help handling encrypted traffic and media streams.

The processor has rich advanced network and peripheral interfaces, including a 10/100 Ethernet MAC with RMII interface, dual USB 2.0 high-speed ports (one OTG and one HOST), three SDIOs with multi-standard memory card controller, five UART interfaces, five I2C interfaces, one high-speed SPI interface and seven PWMs.

Standard development environment utilizing GNU/GCC Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

2. Features Summary



CPU Sub-system

- Quad core ARM Cortex-A9r4 CPU up to 2GHz (DVFS) and 20,000DMIPS
- ARMv7 instruction set, multi-issue superscalar, out-of-order architecture with dynamic branch prediction
- 32KB instruction cache and 32KB data cache
- 1MB Unified L2 cache
- Advanced NEON and VFP co-processor
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

3D Graphics Processing Unit

- Eight core ARM Mali-450 GPU up to 600MHz+ (DVFS)
- Dual Geometry Processors with 32KB L2 cache
- Six Pixel Processors with 2x 128KB L2 caches
- Concurrent multi-core processing
- 3600Mpix/sec and 132Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support

2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter
- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

Crypto Engine

- Supports AES block cipher with 128/192/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- Supports DES/3DES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- Built-in LSFR Random number generator

Video/Picture CODEC

- Tri-cores Amlogic Video Engine (AVE) based on scalable multi-core architecture with dedicated hardware decoders an encoders
- Hardware based trusted video path (TVP)
- Supports multiple “secured” video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
    - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
    - H.264 MVC up to 1080P@60fps
    - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
    - WMV/VC-1 SP/MP/AP up to 1080P@60fps
    - AVS JiZhun Profile up to 1080P@60fps
    - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
    - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
    - RealVideo 8/9/10 up to 1080P
    - H.265 HEVC up to 720P
    - WebM up to VGA
    - Multiple language and multiple format sub-title video support
    - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
    - Supports JPEG thumbnail, scaling, rotation and transition effects
    - Supports *.mkv,*.wmv,*.mpg, *.mpeg, *.dat, *.avi, *.mov, *.iso, *.mp4, *.rm and *.jpg file formats
- Video/Picture Encoding
    - Independent JPEG and H.264 encoder with configurable performance/bit-rate
    - JPEG image encoding
    - H.264 video encoding up to 1080P@30fps

Video Post-Processing Engine

- Motion adaptive 3D noise reduction filter
- Advanced motion adaptive edge enhancing de-interlacing engine
- 3:2 pull-down support
- Programmable poly-phase scalar for both horizontal and vertical dimension for zoom and windowing
- Programmable color management filter (to enhance blue, green, red, face and other colors)
- Dynamic Non-Linear Luma filter
- Programmable color matrix pipeline
- Video mixer: 2 video planes and 2 graphics planes per video output

Video Output

- Built-in HDMI 1.4b transmitter including both controller and PHY with CEC and HDCP, 4Kx2K@30 max resolution output
- CVBS 480i/576i standard definition output
- Supports all standard SD/HD/UHD video output formats: 480i/p, 576i/p, 720p ,1080i/p and 4Kx2K
- Supports dual video output with combination of CVBS+HDMI
- Supports 3D HDMI display

Audio CODEC and Input/Output

- Low power MediaCPU with DSP audio processing
- Supports MP3, AAC, WMA, RM, FLAC, Ogg and programmable with 5.1 down-mixing
- Internal audio CODEC supporting 3 channels stereo input, 1 channel stereo HP/SPK output and 1 channel 2G mono output
- I2S audio interface supporting 6-channel(5.1) out and 2-channel in
- Built-in SPDIF/IEC958 and PCM serial digital audio input/output
- Supports concurrent dual audio stereo channel output with combination of analog+PCM or I2S+PCM

Memory and Storage Interface

- Dual-channel 32-bit SDRAM memory interface running up to DDR1600
- Supports up to 4GB DDR3, DDR3L, LPDDR2 and LPDDR3 memory
- TrustZone protected DRAM memory region and internal SRAM
- Supports SLC/MLC/TLC NAND Flash with 60-bit ECC, compatible to ONFI 2.1 and Toggle 2.0 mode
- SDSC/SDHC/SDXC card and SDIO interface with 1-bit and 4-bit data bus width supporting spec version 2.x/3.x/4.x DS/HS modes up to UHS-I SDR50
- eMMC and MMC card interface with 1/4/8-bit data bus width supporting spec version 4.4x/4.5x HS200 (up to 100MHz clock), compatible with standard iNAND interface
- Supports serial 1, 2 or 4-bit NOR Flash via SPI interface
- Built-in 4k bits One-Time-Programming ROM for key storage

Network

- Integrated IEEE 802.3 10/100 Ethernet controller with RMII interface
- Optional 50MHz clock output to Ethernet PHY
- WiFi/IEEE802.11 & Bluetooth supporting via SDIO/USB/UART/PCM

Digital Television Interface

- Two transport stream(TS) input interfaces with three built-in demux processor for connecting to external digital TV tuner/demodulator and one output TS interface
- Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
- Integrated CI+ ports and ISO 7816 smart card controller

Integrated I/O Controllers and Interfaces

- Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
- 5 UART, 5 I2C and SPI interface with 3 slave selects
- Seven PWMs
- Programmable IR remote input/output controllers
- Built-in 10bit SAR ADC with 4 input channels
- A set of General Purpose IO interfaces with built-in pull up and pull down

System, Peripherals and Misc. Interfaces

- Integrated general purpose timers, counters, DMA controllers
- Integrated RTC with battery backup option
- 24 MHz and 32 KHz crystal oscillator input
- Embedded debug interface using ICE/JTAG

Power Management

- Multiple external power domains controlled by PMIC
- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs for DVFS operation
- Multi-voltage I/O design for 1.8V and 3.3V
- Power management auxiliary processor in dedicated always-on (AO) power domain to communicate with external PMIC

Security

- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, OTP, internal control buses and storage
- Protected memory regions and scrambled memory data interface
- Trusted Video Path and Secured (needs SecureOS software)

Package

- LFBGA, 19x19mm, 531-ball, 0.65 ball pitch, RoHS compliant

3. Pin Out Specification

3.1 Pin-Out Diagram (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	VDDCPU	GPIOX_12	GPIOX_10	X	X	CARD_2	VDDCPU	X	X	GPIODV_6	GPIODV_8	X	X	GPIODV_21	GPIODV_23	X	X	USBA_VBUS	USBA_DP	X	X	EXTC_HPLL	GPIOH_4	X	X	HDMITX_1P	HDMITX_0P	HDMITX_CKP	A
B	DVSS	GPIOX_11	GPIOX_9	GPIOX_7	CARD_0	CARD_1	CARD_4	CARD_6	GPIODV_3	GPIODV_5	GPIODV_9	GPIODV_16	GPIODV_18	GPIODV_20	EXTC_DPLL	SARADC_CH3	SARADC_CH1	USBA_ID	USBA_DM	CVBS_IOUT	CVBS_RSET	GPIOH_9	GPIOH_3	GPIOH_1	HDMITX_2P	HDMITX_1N	HDMITX_0N	HDMITX_CKN	B
C	GPIOX_18	GPIOX_17	GPIOX_8	GPIOX_6	DVSS	CARD_3	CARD_5	GPIODV_2	GPIODV_4	GPIODV_7	VDDCPU	GPIODV_17	GPIODV_19	GPIODV_22	RREF_DPLL	SARADC_CH2	SARADC_CH0	USBA_TXRTUNE	USBB_TXRTUNE	CVBS_VREF	CVBS_COMP	GPIOH_8	GPIOH_2	GPIOH_0	HDMITX_2N	HDMI_REXT	DVSS	VDDEE_0V9	C
D	X	GPIOX_20	GPIOX_19	VDDCPU	GPIOX_5	X	VDDCPU	X	GPIOX_0	X	DVSS	X	GPIODV_15	X	GPIODV_25	X	GPIODV_29	X	DVSS	X	USBB_VBUS	X	GPIOH_7	VDDEE_0V9	DVSS	XTAL24_xo	HDMI_CEXT	X	D
E	X	GPIOY_4	GPIOX_21	GPIOX_14	GPIOX_13	GPIOX_4	GPIOX_3	GPIOX_2	GPIOX_1	GPIODV_10	GPIODV_11	GPIODV_13	GPIODV_14	GPIODV_24	GPIODV_26	GPIODV_27	SARADC_AVSS18	SARADC_AOUT	USBB_DM	USBB_DP	AVDD18_HPLL	AVSS18_HPLL	GPIOH_6	GPIOH_5	VDDIO_H	X	XTAL24_xi	X	E
F	GPIOY_7	GPIOY_6	GPIOY_5	GPIOX_15	GPIOX_16	X	X	DVSS	GPIODV_0	GPIODV_1	GPIODV_12	VDDIO_CARD	VDDIO_DV	VDDIO_Z	GPIODV_28	USB_VDD33	VDDIO_XTAL_18	SARADC_AVDD18	USB_VDD18	CVBS_AVDD18	HDMITX_AVSS	HDMITX_AVSS	X	HDMITX_AVDD18	X	HDMI_AVSS18	NC1	NC2	F
G	VDDCPU	GPIOY_9	GPIOY_8	X	GPIOY_0	GPIOY_1	X	X	X	VDDCPU	X	DVSS	X	VDDCPU	X	DVSS	X	USB_VSSA	X	CVBS_AVSS	X	X	X	AVDD18	AVDD18	NC5	NC4	NC3	G
H	X	GPIOY_11	GPIOY_10	DVSS	VDDCPU	GPIOY_2	X	X	VDDCPU	X	VDDCPU	X	VDDCPU	X	VDDEE_0V9	X	VDDEE_0V9	X	VDDEE_0V9	X	X	X	HDMI_AVDD18	CSI_0_n	X	NC7	NC6	X	H
J	X	BOOT_18	GPIOY_12	X	GPIOY_13	GPIOY_3	VDDCPU	X													DVSS	X	CSI_0_p	CSI_1_p	CSI_1_n	NC9	NC8	X	J
K	BOOT_15	BOOT_16	BOOT_17	GPIOY_14	GPIOY_16	GPIOY_15	X	VDDCPU		X	DVSS	X	DVSS	X	DVSS	X	DVSS	X	X		X	AVSS	CSI_2_p	CSI_2_n	X	NC11	NC10	DVSS	K
L	BOOT_9	BOOT_8	BOOT_10	X	BOOT_14	VDDIO_Y	DVSS	X		DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		AVSS	X	AVSS	CSI_3_p	CSI_3_n	NC13	NC14	NC12	L
M	X	BOOT_6	BOOT_7	BOOT_13	BOOT_11	BOOT_12	X	VDDCPU		X	VDDCPU	X	VDDCPU	X	DVSS	X	VDDEE_0V9	X	DVSS		X	CSI_AVDD18	CSI_4_p	CSI_4_n	X	GPIOZ_1	GPIOZ_0	X	M
N	X	BOOT_4	BOOT_5	X	BOOT_3	VDDIO_BOOT	VDDCPU	X		DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		VDDEE_0V9	X	CSI_AVSS	CSI_5_p	CSI_5_n	GPIOZ_3	GPIOZ_2	X	N
P	micbias	BSD_EN	DVSS	BOOT_1	BOOT_2	VDDIO_X	X	VDDEE_0V9		X	DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS		X	CSI_AVSS	GPIOZ_9	GPIOZ_10	X	GPIOZ_6	GPIOZ_4	GPIOZ_5	P
R	ainl3	ainl1p	ainl2p	X	BOOT_0	ainr1p	IOVREF_1V8	X		DVSS	X	DVSS	X	VDDEE_0V9	X	DVSS	X	VDDEE_0V9	X		VDDCORE_AO	X	GPIOZ_11	GPIOZ_12	DVSS	GPIOAO_0	GPIOAO_8	GPIOZ_7	R
T	X	vcm	ainl1n	ainr1n	ainr2p	ainr3	X	VDDEE_0V9		X	VDDEE_0V9	X	DVSS	X	DVSS	X	DVSS	X	DVSS		X	EFUSE_VD1V8	GPIOZ_14	GPIOZ_13	X	GPIOAO_2	GPIOAO_1	X	T
U	X	vrefdac	vrefadc	X	lineoutl	lineoutr	DVSS	X		DVSS	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		DVSS	X	GPIOAO_7	GPIOAO_9	GPIOAO_8	GPIOAO_4	GPIOAO_3	X	U
V	avddhs	avdd	vrefn	agnd	lineoutmp	agndhs	X	VDDQ		X	DVSS	X	VDDEE_0V9	X	DVSS	X	VDDEE_0V9	X	DVSS		X	PLL_VDD	GPIOAO_11	GPIOAO_10	X	TEST_N	GPIOAO_5	GPIOAO_6	V
W	hsoutr	vcmbuf	hsoutl	X	lineoutmn	a_DQ15	PLL_VDD	X		X	X	DVSS	X	DVSS	X	DVSS	X	DVSS	X		VDDEE_0V9	X	VDDIO_AO	GPIOAO_13	GPIOAO_12	RTC32k_xo	RTC_VDD_09	RESET_N	W
Y	X	a_DQ3	a_DQ4	a_DQ14	DVSS	a_DQ8	X	VDDEE_0V9													X	VDDQ	b_DQ8	b_DQ15	X	RTC_VSS	RTC32k_xi	X	Y
AA	X	a_DQ5	a_DQ2	X	a_DQ9	VDDQ	X	X	X	DVSS	X	VDDEE_0V9	X	DVSS	X	VDDEE_0V9	X	DVSS	X	b_DTO0	X	X	b_DQ14	b_DQ9	DVSS	b_DQ3	b_DQ4	X	AA
AB	a_DQS0_N	a_DQS0	a_DQM0	a_DQS1	a_DQS1_N	X	X	X	VDDQ	X	VDDQ	X	VDDQ	X	PLL_VSS	X	VDDQ	X	VDDQ	X	X	X	b_DQS1_N	b_DQM1	X	b_DQ5	b_DQ2	DVSS	AB
AC	DVSS	a_DQ6	a_DQ1	X	a_DQM1	X	a_CAS_N	a_CS_N	a_WE_N	a_DQ31	a_DQ30	a_DQM3	a_DQ29	a_DQ28	b_DQ16	b_DQ22	b_DQM2	b_DQ21	b_DQ20	b_WE_N	b_A10	X	X	b_DQS1	b_DQ13	b_DQM0	b_DQS0	b_DQS0_N	AC
AD	X	a_DQ0	a_DQ10	a_DQ13	DVSS	a_ODT	a_CKE	a_A10	a_A15	a_DQ24	a_DQ25	a_DQS3	a_DQ26	DVSS	b_DQ23	b_DQS2	b_DQS2_N	b_DQ18	b_DQ19	DVSS	b_CKE	b_CS_N	b_ODT	DVSS	b_DQ12	b_DQ1	b_DQ6	X	AD
AE	X	a_DQ7	a_DQ11	VDDQ	a_DQ12	a_RAS_N	X	DVSS	X	VDDQ	X	a_DQS3_N	X	a_DQ27	X	b_DQ17	X	VDDQ	X	b_A15	X	b_CAS_N	X	b_RAS_N	VDDQ	b_DQ0	b_DQ10	X	AE
AF	a_A8	a_PZQ	a_A11	a_BA_1	a_CK_N	a_BA_2	a_A0	a_A13	a_A7	a_DQ20	a_DQ18	a_DQS2	a_DQ17	a_DQ16	b_DQ27	b_DQM3	b_DQS3_N	b_DQ30	b_DQ31	b_A14	b_A4	b_BA_1	b_BA_0	b_A3	b_A2	b_A13	b_DQ11	b_DQ7	AF
AG	a_A6	DVSS	a_A1	a_A12	a_CK	a_BA_0	a_A9	a_A5	a_PVREF	a_DQ19	a_DQM2	a_DQS2_N	a_DQ22	a_DQ23	b_DQ29	b_DQS3	b_DQ25	b_DQ24	b_A6	b_A11	b_A1	b_BA_2	b_CK	b_A0	b_A9	b_A5	DVSS	b_PZQ	AG
AH	VDDQ	a_A14	a_A4	X	X	a_A3	a_A2	X	X	DVSS	a_DQ21	X	X	b_DQ28	b_DQ26	X	X	DVSS	b_A8	X	X	b_A12	b_CK_N	X	X	b_A7	b_PVREF	VDDQ	AH
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

3.2 Pin Order

Table 1. Pin Order

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
A1	VDDCPU	B28	HDMITX_CKN	D25	DVSS
A2	GPIOX_12	C1	GPIOX_18	D26	XTAL24_xo
A3	GPIOX_10	C2	GPIOX_17	D27	HDMI_CEXT
A6	CARD_2	C3	GPIOX_8	E2	GPIOY_4
A7	VDDCPU	C4	GPIOX_6	E3	GPIOX_21
A10	GPIODV_6	C5	DVSS	E4	GPIOX_14
A11	GPIODV_8	C6	CARD_3	E5	GPIOX_13
A14	GPIODV_21	C7	CARD_5	E6	GPIOX_4
A15	GPIODV_23	C8	GPIODV_2	E7	GPIOX_3
A18	USBA_VBUS	C9	GPIODV_4	E8	GPIOX_2
A19	USBA_DP	C10	GPIODV_7	E9	GPIOX_1
A22	EXTC_HPLL	C11	VDDCPU	E10	GPIODV_10
A23	GPIOH_4	C12	GPIODV_17	E11	GPIODV_11
A26	HDMITX_1P	C13	GPIODV_19	E12	GPIODV_13
A27	HDMITX_0P	C14	GPIODV_22	E13	GPIODV_14
A28	HDMITX_CKP	C15	RREF_DPLL	E14	GPIODV_24
B1	DVSS	C16	SARADC_CH2	E15	GPIODV_26
B2	GPIOX_11	C17	SARADC_CH0	E16	GPIODV_27
B3	GPIOX_9	C18	USBA_TXRTUNE	E17	SARADC_AVSS18
B4	GPIOX_7	C19	USBB_TXRTUNE	E18	SARADC_AOUT
B5	CARD_0	C20	CVBS_VREF	E19	USBB_DM
B6	CARD_1	C21	CVBS_COMP	E20	USBB_DP
B7	CARD_4	C22	GPIOH_8	E21	AVDD18_HPLL
B8	CARD_6	C23	GPIOH_2	E22	AVSS18_HPLL
B9	GPIODV_3	C24	GPIOH_0	E23	GPIOH_6
B10	GPIODV_5	C25	HDMITX_2N	E24	GPIOH_5
B11	GPIODV_9	C26	HDMI_REXT	E25	VDDIO_H
B12	GPIODV_16	C27	DVSS	E27	XTAL24_xi
B13	GPIODV_18	C28	VDDEE_0V9	F1	GPIOY_7
B14	GPIODV_20	D2	GPIOX_20	F2	GPIOY_6
B15	EXTC_DPLL	D3	GPIOX_19	F3	GPIOY_5
B16	SARADC_CH3	D4	VDDCPU	F4	GPIOX_15
B17	SARADC_CH1	D5	GPIOX_5	F5	GPIOX_16
B18	USBA_ID	D7	VDDCPU	F8	DVSS
B19	USBA_DM	D9	GPIOX_0	F9	GPIODV_0
B20	CVBS_IOUT	D11	DVSS	F10	GPIODV_1
B21	CVBS_RSET	D13	GPIODV_15	F11	GPIODV_12
B22	GPIOH_9	D15	GPIODV_25	F12	VDDIO_CARD
B23	GPIOH_3	D17	GPIODV_29	F13	VDDIO_DV
B24	GPIOH_1	D19	DVSS	F14	VDDIO_Z
B25	HDMITX_2P	D21	USBB_VBUS	F15	GPIODV_28
B26	HDMITX_1N	D23	GPIOH_7	F16	USB_VDD33
B27	HDMITX_0N	D24	VDDEE_0V9	F17	VDDIO_XTAL_18

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
F18	SARADC_AVDD18	J23	CSI_0_p	M11	VDDCPU
F19	USB_VDD18	J24	CSI_1_p	M13	VDDCPU
F20	CVBS_AVDD18	J25	CSI_1_n	M15	DVSS
F21	HDMITX_AVSS	J26	NC9	M17	VDDEE_0V9
F22	HDMITX_AVSS	J27	NC8	M19	DVSS
F24	HDMITX_AVDD18	K1	BOOT_15	M22	CSI_AVDD18
F26	HDMI_AVSS18	K2	BOOT_16	M23	CSI_4_p
F27	NC1	K3	BOOT_17	M24	CSI_4_n
F28	NC2	K4	GPIOY_14	M26	GPIOZ_1
G1	VDDCPU	K5	GPIOY_16	M27	GPIOZ_0
G2	GPIOY_9	K6	GPIOY_15	N2	BOOT_4
G3	GPIOY_8	K8	VDDCPU	N3	BOOT_5
G5	GPIOY_0	K11	DVSS	N5	BOOT_3
G6	GPIOY_1	K13	DVSS	N6	VDDIO_BOOT
G10	VDDCPU	K15	DVSS	N7	VDDCPU
G12	DVSS	K17	DVSS	N10	DVSS
G14	VDDCPU	K22	AVSS	N12	DVSS
G16	DVSS	K23	CSI_2_p	N14	DVSS
G18	USB_VSSA	K24	CSI_2_n	N16	DVSS
G20	CVBS_AVSS	K26	NC11	N18	DVSS
G24	AVDD18	K27	NC10	N21	VDDEE_0V9
G25	AVDD18	K28	DVSS	N23	CSI_AVSS
G26	NC5	L1	BOOT_9	N24	CSI_5_p
G27	NC4	L2	BOOT_8	N25	CSI_5_n
G28	NC3	L3	BOOT_10	N26	GPIOZ_3
H2	GPIOY_11	L5	BOOT_14	N27	GPIOZ_2
H3	GPIOY_10	L6	VDDIO_Y	P1	micbias
H4	DVSS	L7	DVSS	P2	BSD_EN
H5	VDDCPU	L10	DVSS	P3	DVSS
H6	GPIOY_2	L12	DVSS	P4	BOOT_1
H9	VDDCPU	L14	DVSS	P5	BOOT_2
H11	VDDCPU	L16	DVSS	P6	VDDIO_X
H13	VDDCPU	L18	DVSS	P8	VDDEE_0V9
H15	VDDEE_0V9	L21	AVSS	P11	DVSS
H17	VDDEE_0V9	L23	AVSS	P13	DVSS
H19	VDDEE_0V9	L24	CSI_3_p	P15	DVSS
H23	HDMI_AVDD18	L25	CSI_3_n	P17	DVSS
H24	CSI_0_n	L26	NC13	P19	DVSS
H26	NC7	L27	NC14	P22	CSI_AVSS
H27	NC6	L28	NC12	P23	GPIOZ_9
J2	BOOT_18	M2	BOOT_6	P24	GPIOZ_10
J3	GPIOY_12	M3	BOOT_7	P26	GPIOZ_6
J5	GPIOY_13	M4	BOOT_13	P27	GPIOZ_4
J6	GPIOY_3	M5	BOOT_11	P28	GPIOZ_5
J7	VDDCPU	M6	BOOT_12	R1	ainl3
J21	DVSS	M8	VDDCPU	R2	ainl1p

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
R3	ainl2p	U26	GPIOAO_4	Y26	RTC_VSS
R5	BOOT_0	U27	GPIOAO_3	Y27	RTC32k_xi
R6	ainr1p	V1	avddhs	AA2	a_DQ5
R7	IOVREF_1V8	V2	avdd	AA3	a_DQ2
R10	DVSS	V3	vrefn	AA5	a_DQ9
R12	DVSS	V4	agnd	AA6	VDDQ
R14	VDDEE_0V9	V5	lineoutmp	AA10	DVSS
R16	DVSS	V6	agndhs	AA12	VDDEE_0V9
R18	VDDEE_0V9	V8	VDDQ	AA14	DVSS
R21	VDDCORE_AO	V11	DVSS	AA16	VDDEE_0V9
R23	GPIOZ_11	V13	VDDEE_0V9	AA18	DVSS
R24	GPIOZ_12	V15	DVSS	AA20	b_DTO0
R25	DVSS	V17	VDDEE_0V9	AA23	b_DQ14
R26	GPIOAO_0	V19	DVSS	AA24	b_DQ9
R27	GPIOZ_8	V22	PLL_VDD	AA25	DVSS
R28	GPIOZ_7	V23	GPIOAO_11	AA26	b_DQ3
T2	vcm	V24	GPIOAO_10	AA27	b_DQ4
T3	ainl1n	V26	TEST_N	AB1	a_DQS0_N
T4	ainr1n	V27	GPIOAO_5	AB2	a_DQS0
T5	ainr2p	V28	GPIOAO_6	AB3	a_DQM0
T6	ainr3	W1	hsoutr	AB4	a_DQS1
T8	VDDEE_0V9	W2	vcmbuf	AB5	a_DQS1_N
T11	VDDEE_0V9	W3	hsoutl	AB9	VDDQ
T13	DVSS	W5	lineoutmn	AB11	VDDQ
T15	DVSS	W6	a_DQ15	AB13	VDDQ
T17	DVSS	W7	PLL_VDD	AB15	PLL_VSS
T19	DVSS	W12	DVSS	AB17	VDDQ
T22	EFUSE_VDD1V8	W14	DVSS	AB19	VDDQ
T23	GPIOZ_14	W16	DVSS	AB23	b_DQS1_N
T24	GPIOZ_13	W18	DVSS	AB24	b_DQM1
T26	GPIOAO_2	W21	VDDEE_0V9	AB26	b_DQ5
T27	GPIOAO_1	W23	VDDIO_AO	AB27	b_DQ2
U2	vrefdac	W24	GPIOAO_13	AB28	DVSS
U3	vrefadc	W25	GPIOAO_12	AC1	DVSS
U5	lineoutl	W26	RTC32k_xo	AC2	a_DQ6
U6	lineoutr	W27	RTC_VDD_0.9	AC3	a_DQ1
U7	DVSS	W28	RESET_N	AC5	a_DQM1
U10	DVSS	Y2	a_DQ3	AC7	a_CAS_N
U12	DVSS	Y3	a_DQ4	AC8	a_CS_N
U14	DVSS	Y4	a_DQ14	AC9	a_WE_N
U16	DVSS	Y5	DVSS	AC10	a_DQ31
U18	DVSS	Y6	a_DQ8	AC11	a_DQ30
U21	DVSS	Y8	VDDEE_0V9	AC12	a_DQM3
U23	GPIOAO_7	Y22	VDDQ	AC13	a_DQ29
U24	GPIOAO_9	Y23	b_DQ8	AC14	a_DQ28
U25	GPIOAO_8	Y24	b_DQ15	AC15	b_DQ16

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
AC16	b_DQ22	AE8	DVSS	AG3	a_A1
AC17	b_DQM2	AE10	VDDQ	AG4	a_A12
AC18	b_DQ21	AE12	a_DQS3_N	AG5	a_CK
AC19	b_DQ20	AE14	a_DQ27	AG6	a_BA_0
AC20	b_WE_N	AE16	b_DQ17	AG7	a_A9
AC21	b_A10	AE18	VDDQ	AG8	a_A5
AC24	b_DQS1	AE20	b_A15	AG9	a_PVREF
AC25	b_DQ13	AE22	b_CAS_N	AG10	a_DQ19
AC26	b_DQM0	AE24	b_RAS_N	AG11	a_DQM2
AC27	b_DQS0	AE25	VDDQ	AG12	a_DQS2_N
AC28	b_DQS0_N	AE26	b_DQ0	AG13	a_DQ22
AD2	a_DQ0	AE27	b_DQ10	AG14	a_DQ23
AD3	a_DQ10	AF1	a_A8	AG15	b_DQ29
AD4	a_DQ13	AF2	a_PZQ	AG16	b_DQS3
AD5	DVSS	AF3	a_A11	AG17	b_DQ25
AD6	a_ODT	AF4	a_BA_1	AG18	b_DQ24
AD7	a_CKE	AF5	a_CK_N	AG19	b_A6
AD8	a_A10	AF6	a_BA_2	AG20	b_A11
AD9	a_A15	AF7	a_A0	AG21	b_A1
AD10	a_DQ24	AF8	a_A13	AG22	b_BA_2
AD11	a_DQ25	AF9	a_A7	AG23	b_CK
AD12	a_DQS3	AF10	a_DQ20	AG24	b_A0
AD13	a_DQ26	AF11	a_DQ18	AG25	b_A9
AD14	DVSS	AF12	a_DQS2	AG26	b_A5
AD15	b_DQ23	AF13	a_DQ17	AG27	DVSS
AD16	b_DQS2	AF14	a_DQ16	AG28	b_PZQ
AD17	b_DQS2_N	AF15	b_DQ27	AH1	VDDQ
AD18	b_DQ18	AF16	b_DQM3	AH2	a_A14
AD19	b_DQ19	AF17	b_DQS3_N	AH3	a_A4
AD20	DVSS	AF18	b_DQ30	AH6	a_A3
AD21	b_CKE	AF19	b_DQ31	AH7	a_A2
AD22	b_CS_N	AF20	b_A14	AH10	DVSS
AD23	b_ODT	AF21	b_A4	AH11	a_DQ21
AD24	DVSS	AF22	b_BA_1	AH14	b_DQ28
AD25	b_DQ12	AF23	b_BA_0	AH15	b_DQ26
AD26	b_DQ1	AF24	b_A3	AH18	DVSS
AD27	b_DQ6	AF25	b_A2	AH19	b_A8
AE2	a_DQ7	AF26	b_A13	AH22	b_A12
AE3	a_DQ11	AF27	b_DQ11	AH23	b_CK_N
AE4	VDDQ	AF28	b_DQ7	AH26	b_A7
AE5	a_DQ12	AG1	a_A6	AH27	b_PVREF
AE6	a_RAS_N	AG2	DVSS	AH28	VDDQ

3.3 Pin Description

The S802 application processor pin assignment is described in the following table.

Table 2. Pin Name assignments

Net Name	Type	Default Pull UP/DN	Description	Power Domain
GPIOX - Refer to Table 3 for functional multiplex information.				
GPIOX_0	DIO	UP	General purpose input/output bank X signal 0	VDDIO_X
GPIOX_1	DIO	UP	General purpose input/output bank X signal 1	VDDIO_X
GPIOX_2	DIO	UP	General purpose input/output bank X signal 2	VDDIO_X
GPIOX_3	DIO	UP	General purpose input/output bank X signal 3	VDDIO_X
GPIOX_4	DIO	UP	General purpose input/output bank X signal 4	VDDIO_X
GPIOX_5	DIO	UP	General purpose input/output bank X signal 5	VDDIO_X
GPIOX_6	DIO	UP	General purpose input/output bank X signal 6	VDDIO_X
GPIOX_7	DIO	UP	General purpose input/output bank X signal 7	VDDIO_X
GPIOX_8	DIO	UP	General purpose input/output bank X signal 8	VDDIO_X
GPIOX_9	DIO	UP	General purpose input/output bank X signal 9	VDDIO_X
GPIOX_10	DIO	UP	General purpose input/output bank X signal 10	VDDIO_X
GPIOX_11	DIO	UP	General purpose input/output bank X signal 11	VDDIO_X
GPIOX_12	DIO	UP	General purpose input/output bank X signal 12	VDDIO_X
GPIOX_13	DIO	UP	General purpose input/output bank X signal 13	VDDIO_X
GPIOX_14	DIO	UP	General purpose input/output bank X signal 14	VDDIO_X
GPIOX_15	DIO	UP	General purpose input/output bank X signal 15	VDDIO_X
GPIOX_16	DIO	UP	General purpose input/output bank X signal 16	VDDIO_X
GPIOX_17	DIO	UP	General purpose input/output bank X signal 17	VDDIO_X
GPIOX_18	DIO	DOWN	General purpose input/output bank X signal 18	VDDIO_X
GPIOX_19	DIO	UP	General purpose input/output bank X signal 19	VDDIO_X
GPIOX_20	DIO	DOWN	General purpose input/output bank X signal 20	VDDIO_X
GPIOX_21	DIO	UP	General purpose input/output bank X signal 21	VDDIO_X
VDDIO_X	P	-	Power supply for GPIO bank X	-
GPIOY - Refer to Table 4 for functional multiplex information.				
GPIOY_0	DIO	UP	General purpose input/output bank Y signal 0	VDDIO_Y
GPIOY_1	DIO	UP	General purpose input/output bank Y signal 1	VDDIO_Y
GPIOY_2	DIO	UP	General purpose input/output bank Y signal 2	VDDIO_Y
GPIOY_3	DIO	UP	General purpose input/output bank Y signal 3	VDDIO_Y
GPIOY_4	DIO	UP	General purpose input/output bank Y signal 4	VDDIO_Y
GPIOY_5	DIO	UP	General purpose input/output bank Y signal 5	VDDIO_Y
GPIOY_6	DIO	UP	General purpose input/output bank Y signal 6	VDDIO_Y
GPIOY_7	DIO	UP	General purpose input/output bank Y signal 7	VDDIO_Y
GPIOY_8	DIO	UP	General purpose input/output bank Y signal 8	VDDIO_Y
GPIOY_9	DIO	UP	General purpose input/output bank Y signal 9	VDDIO_Y
GPIOY_10	DIO	UP	General purpose input/output bank Y signal 10	VDDIO_Y
GPIOY_11	DIO	UP	General purpose input/output bank Y signal 11	VDDIO_Y
GPIOY_12	DIO	UP	General purpose input/output bank Y signal 12	VDDIO_Y
GPIOY_13	DIO	UP	General purpose input/output bank Y signal 13	VDDIO_Y
GPIOY_14	DIO	DOWN	General purpose input/output bank Y signal 14	VDDIO_Y
GPIOY_15	DIO	DOWN	General purpose input/output bank Y signal 15	VDDIO_Y

Net Name	Type	Default Pull UP/DN	Description	Power Domain
GPIOY_16	DIO	DOWN	General purpose input/output bank Y signal 16	VDDIO_Y
VDDIO_Y	P	-	Power supply for GPIO bank Y	-
GPIODV - Refer to Table 5 for functional multiplex information.				
GPIODV_0	DIO	DOWN	General purpose input/output bank DV signal 0	VDDIO_DV
GPIODV_1	DIO	DOWN	General purpose input/output bank DV signal 1	VDDIO_DV
GPIODV_2	DIO	DOWN	General purpose input/output bank DV signal 2	VDDIO_DV
GPIODV_3	DIO	DOWN	General purpose input/output bank DV signal 3	VDDIO_DV
GPIODV_4	DIO	DOWN	General purpose input/output bank DV signal 4	VDDIO_DV
GPIODV_5	DIO	DOWN	General purpose input/output bank DV signal 5	VDDIO_DV
GPIODV_6	DIO	DOWN	General purpose input/output bank DV signal 6	VDDIO_DV
GPIODV_7	DIO	DOWN	General purpose input/output bank DV signal 7	VDDIO_DV
GPIODV_8	DIO	DOWN	General purpose input/output bank DV signal 8	VDDIO_DV
GPIODV_9	DIO	DOWN	General purpose input/output bank DV signal 9	VDDIO_DV
GPIODV_10	DIO	DOWN	General purpose input/output bank DV signal 10	VDDIO_DV
GPIODV_11	DIO	DOWN	General purpose input/output bank DV signal 11	VDDIO_DV
GPIODV_12	DIO	DOWN	General purpose input/output bank DV signal 12	VDDIO_DV
GPIODV_13	DIO	DOWN	General purpose input/output bank DV signal 13	VDDIO_DV
GPIODV_14	DIO	DOWN	General purpose input/output bank DV signal 14	VDDIO_DV
GPIODV_15	DIO	DOWN	General purpose input/output bank DV signal 15	VDDIO_DV
GPIODV_16	DIO	DOWN	General purpose input/output bank DV signal 16	VDDIO_DV
GPIODV_17	DIO	DOWN	General purpose input/output bank DV signal 17	VDDIO_DV
GPIODV_18	DIO	DOWN	General purpose input/output bank DV signal 18	VDDIO_DV
GPIODV_19	DIO	DOWN	General purpose input/output bank DV signal 19	VDDIO_DV
GPIODV_20	DIO	DOWN	General purpose input/output bank DV signal 20	VDDIO_DV
GPIODV_21	DIO	DOWN	General purpose input/output bank DV signal 21	VDDIO_DV
GPIODV_22	DIO	DOWN	General purpose input/output bank DV signal 22	VDDIO_DV
GPIODV_23	DIO	DOWN	General purpose input/output bank DV signal 23	VDDIO_DV
GPIODV_24	DIO	DOWN	General purpose input/output bank DV signal 24	VDDIO_DV
GPIODV_25	DIO	DOWN	General purpose input/output bank DV signal 25	VDDIO_DV
GPIODV_26	DIO	DOWN	General purpose input/output bank DV signal 26	VDDIO_DV
GPIODV_27	DIO	DOWN	General purpose input/output bank DV signal 27	VDDIO_DV
GPIODV_28	DIO	DOWN	General purpose input/output bank DV signal 28	VDDIO_DV
GPIODV_29	DIO	UP	General purpose input/output bank DV signal 29	VDDIO_DV
VDDIO_DV	P	-	Power supply for GPIO bank DV	-
CARD - Refer to Table 6 for functional multiplex information.				
CARD_0	DIO	UP	General purpose input/output bank CARD signal 0	VDDIO_CARD
CARD_1	DIO	UP	General purpose input/output bank CARD signal 1	VDDIO_CARD
CARD_2	DIO	UP	General purpose input/output bank CARD signal 2	VDDIO_CARD
CARD_3	DIO	UP	General purpose input/output bank CARD signal 3	VDDIO_CARD
CARD_4	DIO	UP	General purpose input/output bank CARD signal 4	VDDIO_CARD
CARD_5	DIO	UP	General purpose input/output bank CARD signal 5	VDDIO_CARD
CARD_6	DIO	UP	General purpose input/output bank CARD signal 6	VDDIO_CARD
VDDIO_CARD	P	-	Power supply for GPIO bank CARD	-
BOOT - Refer to Table 7 for functional multiplex information.				

Net Name	Type	Default Pull UP/DN	Description	Power Domain
BSD_EN	DIO	DOWN	Boundary Scan Enable signal. Should be kept low during normal operation.	VDDIO_BOOT
BOOT_0	DIO	UP	General purpose input/output bank BOOT signal 0	VDDIO_BOOT
BOOT_1	DIO	UP	General purpose input/output bank BOOT signal 1	VDDIO_BOOT
BOOT_2	DIO	UP	General purpose input/output bank BOOT signal 2	VDDIO_BOOT
BOOT_3	DIO	UP	General purpose input/output bank BOOT signal 3	VDDIO_BOOT
BOOT_4	DIO	UP	General purpose input/output bank BOOT signal 4	VDDIO_BOOT
BOOT_5	DIO	UP	General purpose input/output bank BOOT signal 5	VDDIO_BOOT
BOOT_6	DIO	UP	General purpose input/output bank BOOT signal 6	VDDIO_BOOT
BOOT_7	DIO	UP	General purpose input/output bank BOOT signal 7	VDDIO_BOOT
BOOT_8	DIO	UP	General purpose input/output bank BOOT signal 8	VDDIO_BOOT
BOOT_9	DIO	UP	General purpose input/output bank BOOT signal 9	VDDIO_BOOT
BOOT_10	DIO	UP	General purpose input/output bank BOOT signal 10	VDDIO_BOOT
BOOT_11	DIO	UP	General purpose input/output bank BOOT signal 11	VDDIO_BOOT
BOOT_12	DIO	UP	General purpose input/output bank BOOT signal 12	VDDIO_BOOT
BOOT_13	DIO	UP	General purpose input/output bank BOOT signal 13	VDDIO_BOOT
BOOT_14	DIO	UP	General purpose input/output bank BOOT signal 14	VDDIO_BOOT
BOOT_15	DIO	UP	General purpose input/output bank BOOT signal 15	VDDIO_BOOT
BOOT_16	DIO	UP	General purpose input/output bank BOOT signal 16	VDDIO_BOOT
BOOT_17	DIO	UP	General purpose input/output bank BOOT signal 17	VDDIO_BOOT
BOOT_18	DIO	UP	General purpose input/output bank BOOT signal 18	VDDIO_BOOT
VDDIO_BOOT	P	-	Power supply for GPIO bank BOOT	-
GPIOH - Refer to Table 8 for functional multiplex information.				
GPIOH_0	DIO	UP	General purpose input/output bank H signal 0	VDDIO_H
GPIOH_1	DIO	UP	General purpose input/output bank H signal 1	VDDIO_H
GPIOH_2	DIO	UP	General purpose input/output bank H signal 2	VDDIO_H
GPIOH_3	DIO	UP	General purpose input/output bank H signal 3	VDDIO_H
GPIOH_4	DIO	DOWN	General purpose input/output bank H signal 4	VDDIO_H
GPIOH_5	DIO	DOWN	General purpose input/output bank H signal 5	VDDIO_H
GPIOH_6	DIO	DOWN	General purpose input/output bank H signal 6	VDDIO_H
GPIOH_7	DIO	UP	General purpose input/output bank H signal 7	VDDIO_H
GPIOH_8	DIO	UP	General purpose input/output bank H signal 8	VDDIO_H
GPIOH_9	DIO	UP	General purpose input/output bank H signal 9	VDDIO_H
VDDIO_H	P	-	Power supply for GPIO bank H	-
GPIOZ - Refer to Table 9 for functional multiplex information.				
GPIOZ_0	DIO	DOWN	General purpose input/output bank Z signal 0	VDDIO_Z
GPIOZ_1	DIO	DOWN	General purpose input/output bank Z signal 1	VDDIO_Z
GPIOZ_2	DIO	UP	General purpose input/output bank Z signal 2	VDDIO_Z
GPIOZ_3	DIO	UP	General purpose input/output bank Z signal 3	VDDIO_Z
GPIOZ_4	DIO	UP	General purpose input/output bank Z signal 4	VDDIO_Z
GPIOZ_5	DIO	UP	General purpose input/output bank Z signal 5	VDDIO_Z
GPIOZ_6	DIO	UP	General purpose input/output bank Z signal 6	VDDIO_Z
GPIOZ_7	DIO	UP	General purpose input/output bank Z signal 7	VDDIO_Z
GPIOZ_8	DIO	UP	General purpose input/output bank Z signal 8	VDDIO_Z
GPIOZ_9	DIO	UP	General purpose input/output bank Z signal 9	VDDIO_Z

Net Name	Type	Default Pull UP/DN	Description	Power Domain
GPIOZ_10	DIO	UP	General purpose input/output bank Z signal 10	VDDIO_Z
GPIOZ_11	DIO	UP	General purpose input/output bank Z signal 11	VDDIO_Z
GPIOZ_12	DIO	UP	General purpose input/output bank Z signal 12	VDDIO_Z
GPIOZ_13	DIO	UP	General purpose input/output bank Z signal 13	VDDIO_Z
GPIOZ_14	DIO	UP	General purpose input/output bank Z signal 14	VDDIO_Z
VDDIO_Z	P	-	Power supply for GPIO bank Z	-
GPIOAO - Refer to Table 10 for functional multiplex information.				
GPIOAO_0	DIO	DOWN	General purpose input/output bank AO signal 0	VDDIO_AO
GPIOAO_1	DIO	DOWN	General purpose input/output bank AO signal 1	VDDIO_AO
GPIOAO_2	DIO	DOWN	General purpose input/output bank AO signal 2	VDDIO_AO
GPIOAO_3	DIO	DOWN	General purpose input/output bank AO signal 3	VDDIO_AO
GPIOAO_4	DIO	DOWN	General purpose input/output bank AO signal 4	VDDIO_AO
GPIOAO_5	DIO	DOWN	General purpose input/output bank AO signal 5	VDDIO_AO
GPIOAO_6	DIO	DOWN	General purpose input/output bank AO signal 6	VDDIO_AO
GPIOAO_7	DIO	UP	General purpose input/output bank AO signal 7	VDDIO_AO
GPIOAO_8	DIO	UP	General purpose input/output bank AO signal 8	VDDIO_AO
GPIOAO_9	DIO	UP	General purpose input/output bank AO signal 9	VDDIO_AO
GPIOAO_10	DIO	UP	General purpose input/output bank AO signal 10	VDDIO_AO
GPIOAO_11	DIO	UP	General purpose input/output bank AO signal 11	VDDIO_AO
GPIOAO_12	DIO	UP	General purpose input/output bank AO signal 12	VDDIO_AO
GPIOAO_13	DIO	UP	General purpose input/output bank AO signal 13	VDDIO_AO
TEST_N	DIO	UP	General purpose input/output bank AO signal 14	VDDIO_AO
RESET_N	DI	-	System reset input	VDDIO_AO
VDDIO_AO	P	-	Power supply for GPIO bank AO	-
VDDCORE_AO	P	-	Power supply for Always-On (AO) core logic	-
SARADC				
SARADC_CH0	AI	-	ADC channel 0 input	SARADC_AVDD18
SARADC_CH1	AI	-	ADC channel 1 input	SARADC_AVDD18
SARADC_CH2	AI	-	ADC channel 2 input	SARADC_AVDD18
SARADC_CH3	AI	-	ADC channel 3 input	SARADC_AVDD18
SARADC_AOUT	AO	-	Reserved	SARADC_AVDD18
SARADC_AVDD18	P	-	Analog power supply for ADC & DPLL	-
SARADC_AVSS18	G	-	Analog power ground for ADC & DPLL	-
CVBS				
CVBS_COMP	A	-	CVBS external compensation capacitor connection	CVBS_AVDD18
CVBS_RSET	A	-	CVBS output strength setting resistor	CVBS_AVDD18
CVBS_VREF	A	-	CVBS reference voltage filter cap	CVBS_AVDD18
CVBS_IOUT	AO	-	CVBS output	CVBS_AVDD18
CVBS_AVDD18	P	-	Analog power supply for CVBS	-
CVBS_AVSS	G	-	Analog power ground for CVBS	-
HDMI				
HDMI_CEXT	A	-	HDMI external filter cap	HDMI_AVDD18
HDMI_REXT	A	-	HDMI output strength setting resistor	HDMI_AVDD18
HDMI_AVDD18	P	-	Power supply for HDMI	-
HDMI_AVSS18	G	-	Power ground for HDMI	-

Net Name	Type	Default Pull UP/DN	Description	Power Domain
HDMITX_CKP	AO	-	HDMI TMDS clock positive output	HDMITX_AVDD18
HDMITX_CKN	AO	-	HDMI TMDS clock negative output	HDMITX_AVDD18
HDMITX_0P	AO	-	HDMI TMDS data0 positive output	HDMITX_AVDD18
HDMITX_0N	AO	-	HDMI TMDS data0 negative output	HDMITX_AVDD18
HDMITX_1P	AO	-	HDMI TMDS data1 positive output	HDMITX_AVDD18
HDMITX_1N	AO	-	HDMI TMDS data1 negative output	HDMITX_AVDD18
HDMITX_2P	AO	-	HDMI TMDS data1 positive output	HDMITX_AVDD18
HDMITX_2N	AO	-	HDMI TMDS data1 negative output	HDMITX_AVDD18
HDMITX_AVDD18	P		Power supply for HDMITX	-
HDMITX_AVSS	G		Power ground for HDMITX	-
CSI - Refer to Table 11 for functional multiplex information.				
CSI_0_p	AI	-	TS-in data 0 positive input	CSI_AVDD18
CSI_0_n	AI	-	TS-in data 0 negative input	CSI_AVDD18
CSI_1_p	AI	-	TS-in data 1 positive input	CSI_AVDD18
CSI_1_n	AI	-	TS-in data 1 negative input	CSI_AVDD18
CSI_2_p	AI	-	TS-in data 2 positive input	CSI_AVDD18
CSI_2_n	AI	-	TS-in data 2 negative input	CSI_AVDD18
CSI_3_p	AI	-	TS-in data 3 positive input	CSI_AVDD18
CSI_3_n	AI	-	TS-in data 3 negative input	CSI_AVDD18
CSI_4_p	AI	-	TS-in data 4 positive input	CSI_AVDD18
CSI_4_n	AI	-	TS-in data 4 negative input	CSI_AVDD18
CSI_5_p	AI	-	TS-in data 5 positive input	CSI_AVDD18
CSI_5_n	AI	-	S-in data 5 negative input	CSI_AVDD18
CSI_AVDD18	P	-	Power supply for TSin	-
CSI_AVSS	G	-	Power ground for TSin	-
DRAM				
a_A0	DO	-	DRAM Channel A address bus bit 0	VDDQ
a_A1	DO	-	DRAM Channel A address bus bit 1	VDDQ
a_A2	DO	-	DRAM Channel A address bus bit 2	VDDQ
a_A3	DO	-	DRAM Channel A address bus bit 3	VDDQ
a_A4	DO	-	DRAM Channel A address bus bit 4	VDDQ
a_A5	DO	-	DRAM Channel A address bus bit 5	VDDQ
a_A6	DO	-	DRAM Channel A address bus bit 6	VDDQ
a_A7	DO	-	DRAM Channel A address bus bit 7	VDDQ
a_A8	DO	-	DRAM Channel A address bus bit 8	VDDQ
a_A9	DO	-	DRAM Channel A address bus bit 9	VDDQ
a_A10	DO	-	DRAM Channel A address bus bit 10	VDDQ
a_A11	DO	-	DRAM Channel A address bus bit 11	VDDQ
a_A12	DO	-	DRAM Channel A address bus bit 12	VDDQ
a_A13	DO	-	DRAM Channel A address bus bit 13	VDDQ
a_A14	DO	-	DRAM Channel A address bus bit 14	VDDQ
a_A15	DO	-	DRAM Channel A address bus bit 15	VDDQ
a_BA_0	DO	-	DRAM Channel A bank address bus bit 0	VDDQ
a_BA_1	DO	-	DRAM Channel A bank address bus bit 1	VDDQ
a_BA_2	DO	-	DRAM Channel A bank address bus bit 2	VDDQ

Net Name	Type	Default Pull UP/DN	Description	Power Domain
a_CAS_N	DO	-	DRAM Channel A column address strobe	VDDQ
a_CK	DO	-	DRAM Channel A clock positive output	VDDQ
a_CK_N	DO	-	DRAM Channel A clock negative output	VDDQ
a_CKE	DO	-	DRAM Channel A clock enable output	VDDQ
a_CS_N	DO	-	DRAM Channel A chip select output	VDDQ
a_ODT	DO	-	DRAM Channel A on-die termination	VDDQ
a_RAS_N	DO	-	DRAM Channel A row address strobe	VDDQ
a_WE_N	DO	-	DRAM Channel A write enable	VDDQ
a_DQ0	DIO	-	DRAM Channel A data bus bit 0	VDDQ
a_DQ1	DIO	-	DRAM Channel A data bus bit 1	VDDQ
a_DQ2	DIO	-	DRAM Channel A data bus bit 2	VDDQ
a_DQ3	DIO	-	DRAM Channel A data bus bit 3	VDDQ
a_DQ4	DIO	-	DRAM Channel A data bus bit 4	VDDQ
a_DQ5	DIO	-	DRAM Channel A data bus bit 5	VDDQ
a_DQ6	DIO	-	DRAM Channel A data bus bit 6	VDDQ
a_DQ7	DIO	-	DRAM Channel A data bus bit 7	VDDQ
a_DQ8	DIO	-	DRAM Channel A data bus bit 8	VDDQ
a_DQ9	DIO	-	DRAM Channel A data bus bit 9	VDDQ
a_DQ10	DIO	-	DRAM Channel A data bus bit 10	VDDQ
a_DQ11	DIO	-	DRAM Channel A data bus bit 11	VDDQ
a_DQ12	DIO	-	DRAM Channel A data bus bit 12	VDDQ
a_DQ13	DIO	-	DRAM Channel A data bus bit 13	VDDQ
a_DQ14	DIO	-	DRAM Channel A data bus bit 14	VDDQ
a_DQ15	DIO	-	DRAM Channel A data bus bit 15	VDDQ
a_DQ16	DIO	-	DRAM Channel A data bus bit 16	VDDQ
a_DQ17	DIO	-	DRAM Channel A data bus bit 17	VDDQ
a_DQ18	DIO	-	DRAM Channel A data bus bit 18	VDDQ
a_DQ19	DIO	-	DRAM Channel A data bus bit 19	VDDQ
a_DQ20	DIO	-	DRAM Channel A data bus bit 20	VDDQ
a_DQ21	DIO	-	DRAM Channel A data bus bit 21	VDDQ
a_DQ22	DIO	-	DRAM Channel A data bus bit 22	VDDQ
a_DQ23	DIO	-	DRAM Channel A data bus bit 23	VDDQ
a_DQ24	DIO	-	DRAM Channel A data bus bit 24	VDDQ
a_DQ25	DIO	-	DRAM Channel A data bus bit 25	VDDQ
a_DQ26	DIO	-	DRAM Channel A data bus bit 26	VDDQ
a_DQ27	DIO	-	DRAM Channel A data bus bit 27	VDDQ
a_DQ28	DIO	-	DRAM Channel A data bus bit 28	VDDQ
a_DQ29	DIO	-	DRAM Channel A data bus bit 29	VDDQ
a_DQ30	DIO	-	DRAM Channel A data bus bit 30	VDDQ
a_DQ31	DIO	-	DRAM Channel A data bus bit 31	VDDQ
a_DQM0	DO	-	DRAM Channel A data mask 0	VDDQ
a_DQM1	DO	-	DRAM Channel A data mask 1	VDDQ
a_DQM2	DO	-	DRAM Channel A data mask 2	VDDQ
a_DQM3	DO	-	DRAM Channel A data mask 3	VDDQ
a_DQS0	DIO	-	DRAM Channel A data strobe 0	VDDQ

Net Name	Type	Default Pull UP/DN	Description	Power Domain
a_DQS0_N	DIO	-	DRAM Channel A data strobe 0 complementary	VDDQ
a_DQS1	DIO	-	DRAM Channel A data strobe 0	VDDQ
a_DQS1_N	DIO	-	DRAM Channel A data strobe 0 complementary	VDDQ
a_DQS2	DIO	-	DRAM Channel A data strobe 0	VDDQ
a_DQS2_N	DIO	-	DRAM Channel A data strobe 0 complementary	VDDQ
a_DQS3	DIO	-	DRAM Channel A data strobe 0	VDDQ
a_DQS3_N	DIO	-	DRAM Channel A data strobe 0 complementary	VDDQ
a_PVREF	A	-	DRAM Channel A reference voltage	VDDQ
a_PZQ	A	-	DRAM Channel A reference pin for ZQ calibration	VDDQ
b_A0	DO	-	DRAM Channel B address bus bit 0	VDDQ
b_A1	DO	-	DRAM Channel B address bus bit 1	VDDQ
b_A2	DO	-	DRAM Channel B address bus bit 2	VDDQ
b_A3	DO	-	DRAM Channel B address bus bit 3	VDDQ
b_A4	DO	-	DRAM Channel B address bus bit 4	VDDQ
b_A5	DO	-	DRAM Channel B address bus bit 5	VDDQ
b_A6	DO	-	DRAM Channel B address bus bit 6	VDDQ
b_A7	DO	-	DRAM Channel B address bus bit 7	VDDQ
b_A8	DO	-	DRAM Channel B address bus bit 8	VDDQ
b_A9	DO	-	DRAM Channel B address bus bit 9	VDDQ
b_A10	DO	-	DRAM Channel B address bus bit 10	VDDQ
b_A11	DO	-	DRAM Channel B address bus bit 11	VDDQ
b_A12	DO	-	DRAM Channel B address bus bit 12	VDDQ
b_A13	DO	-	DRAM Channel B address bus bit 13	VDDQ
b_A14	DO	-	DRAM Channel B address bus bit 14	VDDQ
b_A15	DO	-	DRAM Channel B address bus bit 15	VDDQ
b_BA_0	DO	-	DRAM Channel B bank address bus bit 0	VDDQ
b_BA_1	DO	-	DRAM Channel B bank address bus bit 1	VDDQ
b_BA_2	DO	-	DRAM Channel B bank address bus bit 2	VDDQ
b_CAS_N	DO	-	DRAM Channel B column address strobe	VDDQ
b_CK	DO	-	DRAM Channel B clock positive output	VDDQ
b_CK_N	DO	-	DRAM Channel B clock negative output	VDDQ
b_CKE	DO	-	DRAM Channel B clock enable output	VDDQ
b_CS_N	DO	-	DRAM Channel B chip select output	VDDQ
b_ODT	DO	-	DRAM Channel B on-die termination	VDDQ
b_RAS_N	DO	-	DRAM Channel B row address strobe	VDDQ
b_WE_N	DO	-	DRAM Channel B write enable	VDDQ
b_DQ0	DIO	-	DRAM Channel B data bus bit 0	VDDQ
b_DQ1	DIO	-	DRAM Channel B data bus bit 1	VDDQ
b_DQ2	DIO	-	DRAM Channel B data bus bit 2	VDDQ
b_DQ3	DIO	-	DRAM Channel B data bus bit 3	VDDQ
b_DQ4	DIO	-	DRAM Channel B data bus bit 4	VDDQ
b_DQ5	DIO	-	DRAM Channel B data bus bit 5	VDDQ
b_DQ6	DIO	-	DRAM Channel B data bus bit 6	VDDQ
b_DQ7	DIO	-	DRAM Channel B data bus bit 7	VDDQ
b_DQ8	DIO	-	DRAM Channel B data bus bit 8	VDDQ

Net Name	Type	Default Pull UP/DN	Description	Power Domain
b_DQ9	DIO	-	DRAM Channel B data bus bit 9	VDDQ
b_DQ10	DIO	-	DRAM Channel B data bus bit 10	VDDQ
b_DQ11	DIO	-	DRAM Channel B data bus bit 11	VDDQ
b_DQ12	DIO	-	DRAM Channel B data bus bit 12	VDDQ
b_DQ13	DIO	-	DRAM Channel B data bus bit 13	VDDQ
b_DQ14	DIO	-	DRAM Channel B data bus bit 14	VDDQ
b_DQ15	DIO	-	DRAM Channel B data bus bit 15	VDDQ
b_DQ16	DIO	-	DRAM Channel B data bus bit 16	VDDQ
b_DQ17	DIO	-	DRAM Channel B data bus bit 17	VDDQ
b_DQ18	DIO	-	DRAM Channel B data bus bit 18	VDDQ
b_DQ19	DIO	-	DRAM Channel B data bus bit 19	VDDQ
b_DQ20	DIO	-	DRAM Channel B data bus bit 20	VDDQ
b_DQ21	DIO	-	DRAM Channel B data bus bit 21	VDDQ
b_DQ22	DIO	-	DRAM Channel B data bus bit 22	VDDQ
b_DQ23	DIO	-	DRAM Channel B data bus bit 23	VDDQ
b_DQ24	DIO	-	DRAM Channel B data bus bit 24	VDDQ
b_DQ25	DIO	-	DRAM Channel B data bus bit 25	VDDQ
b_DQ26	DIO	-	DRAM Channel B data bus bit 26	VDDQ
b_DQ27	DIO	-	DRAM Channel B data bus bit 27	VDDQ
b_DQ28	DIO	-	DRAM Channel B data bus bit 28	VDDQ
b_DQ29	DIO	-	DRAM Channel B data bus bit 29	VDDQ
b_DQ30	DIO	-	DRAM Channel B data bus bit 30	VDDQ
b_DQ31	DIO	-	DRAM Channel B data bus bit 31	VDDQ
b_DQM0	DO	-	DRAM Channel B data mask 0	VDDQ
b_DQM1	DO	-	DRAM Channel B data mask 1	VDDQ
b_DQM2	DO	-	DRAM Channel B data mask 2	VDDQ
b_DQM3	DO	-	DRAM Channel B data mask 3	VDDQ
b_DQS0	DIO	-	DRAM Channel B data strobe 0	VDDQ
b_DQS0_N	DIO	-	DRAM Channel B data strobe 0 complementary	VDDQ
b_DQS1	DIO	-	DRAM Channel B data strobe 0	VDDQ
b_DQS1_N	DIO	-	DRAM Channel B data strobe 0 complementary	VDDQ
b_DQS2	DIO	-	DRAM Channel B data strobe 0	VDDQ
b_DQS2_N	DIO	-	DRAM Channel B data strobe 0 complementary	VDDQ
b_DQS3	DIO	-	DRAM Channel B data strobe 0	VDDQ
b_DQS3_N	DIO	-	DRAM Channel B data strobe 0 complementary	VDDQ
b_DTO0	DO	-	Test signal	VDDQ
b_PVREF	A	-	DRAM Channel B reference voltage	VDDQ
b_PZQ	A	-	DRAM Channel B reference pin for ZQ calibration	VDDQ
Audio CODEC				
ainl1p	AI	-	Audio stereo line-in 1 left channel	avdd
ainl1n	AI	-	Audio stereo line-in 1 left channel complementary	avdd
ainl2p	AI	-	Audio stereo line-in 2 left channel	avdd
ainr1p	AI	-	Audio stereo line-in 1 right channel	avdd
ainr1n	AI	-	Audio stereo line-in 1 right channel complementary	avdd
ainr2p	AI	-	Audio stereo line-in 2 right channel	avdd

Net Name	Type	Default Pull UP/DN	Description	Power Domain
ainl3	AI	-	Audio stereo line-in 3 left channel	avdd
ainr3	AI	-	Audio stereo line-in 3 left channel	avdd
vcm	A	-	Audio CODEC external filter cap	avdd
vrefadc	A	-	Audio ADC external filter cap	avdd
vrefdac	A	-	Audio DAC external filter cap	avdd
vrefn	A	-	Negative reference, connect to AGND	avdd
micbias	AO	-	Bias voltage output for microphone	avdd
lineoutl	AO	-	Audio stereo line-out left channel	avdd
lineoutr	AO	-	Audio stereo line-out right channel	avdd
lineoutmp	AO	-	Audio mono line-out	avdd
lineoutmn	AO	-	Audio mono line-out complementary	avdd
avdd	P	-	1.8V Power supply for audio CODEC	-
agnd	G	-	Power ground for audio CODEC	-
Headset		-		
hsoutl	AO	-	Headset left channel output	avddhs
hsoutr	AO	-	Headset right channel output	avddhs
vcmbuf	AO	-	Buffered VCM output	avddhs
avddhs	P	-	1.8V Power supply for headset	-
agndhs	G	-	Power ground for headset	-
USB				
USBA_DP	AIO	-	USB OTG positive data signal	USB_VDD33
USBA_DM	AIO	-	USB OTG negative data signal	USB_VDD33
USBA_TXRTUNE	A	-	USB OTG output strength setting resistor	USB_VDD18
USBA_VBUS	AI	-	USB OTG cable power detection (5V tolerance)	USB_VDD18
USBA_ID	DI	-	USB OTG mini-receptacle identifier	USB_VDD18
USBB_DP	AIO	-	USB host positive data signal	USB_VDD33
USBB_DM	AIO	-	USB host negative data signal	USB_VDD33
USBB_TXRTUNE	AIO	-	USB host output strength setting resistor	USB_VDD18
USBB_VBUS	AI	-	USB host cable power detection (5V tolerance)	USB_VDD18
USB_VDD33	P	-	Power supply for USB 3.3V	-
USB_VDD18	P	-	Power supply for USB 1.8V	-
USB_VSSA	G	-	Power ground for headset	-
System Clock & PLL				
XTAL24_xi	AI	-	24MHz crystal oscillator input	VDDIO_XTAL_18
XTAL24_xo	AO	-	24MHz crystal oscillator output	VDDIO_XTAL_18
VDDIO_XTAL_18	P	-	Power supply for 24MHz oscillator	-
RREF_DPLL	A	-	DPLL reference resistor	VDDIO_XTAL_18
EXTC_DPLL	A	-	DPLL external filter cap	VDDIO_XTAL_18
EXTC_HPLL	A	-	HDMI PLL external filter cap	AVDD18_HPLL
AVDD18_HPLL	AP	-	Power supply for HDMI PLL	-
AVSS18_HPLL	G	-	Power ground for HDMI PLL	-
PLL_VDD	P	-	1.8V Power supply for DDR PLL	-
PLL_VSS	P	-	Power ground for PLL	-
RTC32k_xo	DO	-	RTC 32K crystal output	RTC_VDD_0.9
RTC32k_xi	DI	-	RTC 32K crystal input	RTC_VDD_0.9

Net Name	Type	Default Pull UP/DN	Description	Power Domain
RTC_VDD_0.9	P	-	Power supply for RTC	-
RTC_VSS	G	-	Power ground for RTC	-
Digital Power				
VDDCPU	P	-	Power supply for CPU (Cortex A9)	-
VDDQ	P	-	Power supply for DDR	-
VDDEE_0V9	P	-	Power Supply for GPU and core logic	-
IOVREF_1V8	P	-	1.8V Power supply for IOVREF	-
EFUSE_VDD1V8	P	-	1.8V Power supply for EFUSE	-
Digital Ground				
DVSS	P	-	Digital power ground	-

Abbreviations:

- DI = Digital input pin
- DO = Digital output pin
- DIO = Digital input/output pin
- A = Analog setting or filtering pin
- AI = Analog input pin
- AO = Analog output pin
- AIO = Analog input/output pin
- P = Power pin
- AP = Analog power pin
- NC = No connection
- UP = Pull-Up
- DOWN = Pull-down
- Z = Tri-State

3.4 Pin Multiplexing Tables

Multiple usage pins are used to conserve pin consumption for different features. The S802 devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

Table 3. GPIOX_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5
GPIOX_0	SDXC_D0_A/ SD_D0_A	I2C_SDA_C	ENC_0	UART_TX_C	TSout_FAIL
GPIOX_1	SDXC_D1_A/ SD_D1_A	I2C_SCK_C	ENC_1	UART_RX_C	TSout_D_VALID
GPIOX_2	SDXC_D2_A/ SD_D2_A		ENC_2		TSout_SOP
GPIOX_3	SDXC_D3_A/ SD_D3_A		ENC_3		TSout_CLK
GPIOX_4	SDXC_D4_A	PCM_OUT_A	ENC_4	UART_TX_A	TSout_D0
GPIOX_5	SDXC_D5_A	PCM_IN_A	ENC_5	UART_RX_A	TSout_D1
GPIOX_6	SDXC_D6_A	PCM_FS_A	ENC_6	UART_CTS_A	TSout_D2
GPIOX_7	SDXC_D7_A	PCM_CLK_A	ENC_7	UART_RTS_A	TSout_D3
GPIOX_8	SDXC_CLK_A/ SD_CLK_A		ENC_8	TCON_VCOM	TSout_D4
GPIOX_9	SDXC_CMD_A/ SD_CMD_A		ENC_9	PWM_A	TSout_D5
GPIOX_10	XTAL_32K_OUT		ENC_10	PWM_E/ PWM_VS	TSout_D6
GPIOX_11	XTAL_24M/12M_OUT		ENC_11	PWM_B	TSout_D7
GPIOX_12			ENC_12	UART_TX_A	
GPIOX_13			ENC_13	UART_RX_A	
GPIOX_14			END_14	UART_CTS_A	
GPIOX_15			ENC_15	UART_RTS_A	
GPIOX_16			ENC_16		
GPIOX_17			ENC_17		
GPIOX_18					
GPIOX_19					
GPIOX_20				UART_CTS_C	
GPIOX_21				UART_RTS_C	

Table 4. GPIOY_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOY_0	UART_TX_C	I2S_OUT_45	TSin_D_VALID_A	I2C_SDA_C
GPIOY_1	UART_RX_C	I2S_OUT_23	TSin_SOP_A	I2C_SCK_C
GPIOY_2	UART_CTS_C	SPDIF_IN	TSout_CLK	
GPIOY_3	UART_RTS_C	SPDIF_OUT		
GPIOY_4	PCM_OUT_B	I2S_OUT_01	TSin_FAIL_A	
GPIOY_5	PCM_IN_B	I2S_IN_01	TSout_SOP	
GPIOY_6	PCM_FS_B	I2S_LR_CLK	TSout_D_VALID	
GPIOY_7	PCM_CLK_B	I2S_AO_CLK	TSout_FAIL	
GPIOY_8	I2S_AM_CLK		TSin_CLK_A	
GPIOY_9	TSin_D0_A	I2S_OUT_67		
GPIOY_10	TSin_D1_A			
GPIOY_11	TSin_D2_A			
GPIOY_12	TSin_D3_A			
GPIOY_13	TSin_D4_A			
GPIOY_14	TSin_D5_A			
GPIOY_15	TSin_D6_A			
GPIOY_16	TSin_D7_A		PWM_VS	PWM_A

Table 5. GPIODV_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5
GPIODV_0			DVIN_R0	ENC_0	
GPIODV_1			DVIN_R1	ENC_1	
GPIODV_2			DVIN_R2	ENC_2	
GPIODV_3			DVIN_R3	ENC_3	
GPIODV_4			DVIN_R4	ENC_4	
GPIODV_5			DVIN_R5	ENC_5	
GPIODV_6			DVIN_R6	ENC_6	
GPIODV_7			DVIN_R7	ENC_7	
GPIODV_8			DVIN_G0	ENC_8	
GPIODV_9		PWM_VS	DVIN_G1	ENC_9	PWM_C
GPIODV_10			DVIN_G2	ENC_10	
GPIODV_11			DVIN_G3	ENC_11	
GPIODV_12			DVIN_G4	ENC_12	
GPIODV_13			DVIN_G5	ENC_13	
GPIODV_14			DVIN_G6	END_14	
GPIODV_15			DVIN_G7	ENC_15	
GPIODV_16			DVIN_B0	ENC_16	
GPIODV_17			DVIN_B1	ENC_17	
GPIODV_18			DVIN_B2		
GPIODV_19			DVIN_B3		
GPIODV_20			DVIN_B4		
GPIODV_21			DVIN_B5		
GPIODV_22			DVIN_B6		
GPIODV_23			DVIN_B7		
GPIODV_24			DVIN_VS	UART_TX_B	VGA_VS
GPIODV_25			DVIN_HS	UART_RX_B	VGA_HS
GPIODV_26			DVIN_CLK	UART_CTS_B	
GPIODV_27			DVIN_DE	UART_RTS_B	
GPIODV_28	PWM_D	PWM_VS			
GPIODV_29	PWM_C	PWM_VS			

Table 6. CARD_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
CARD_0	SD_D1_B	SDXC_D1_B	JTAG_TDI	
CARD_1	SD_D0_B	SDXC_D0_B	JTAG_TDO	
CARD_2	SD_CLK_B	SDXC_CLK_B	JTAG_CLK	
CARD_3	SD_CMD_B	SDXC_CMD_B	JTAG_TMS	
CARD_4	SD_D3_B	SDXC_D3_B		UART_TX_AO_A
CARD_5	SD_D2_B	SDXC_D2_B		UART_RX_AO_A
CARD_6				

Table 7. BOOT_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
BSD_EN	GPO_BSD (output only)			
BOOT_0	NAND_IO_0	SDXC_D0_C	SD_D0_C	BSD_TDO
BOOT_1	NAND_IO_1	SDXC_D1_C	SD_D1_C	BSD_TDI
BOOT_2	NAND_IO_2	SDXC_D2_C	SD_D2_C	BSD_TMS
BOOT_3	NAND_IO_3	SDXC_D3_C	SD_D3_C	BSD_TCK
BOOT_4	NAND_IO_4	SDXC_D4_C		
BOOT_5	NAND_IO_5	SDXC_D5_C		
BOOT_6	NAND_IO_6	SDXC_D6_C		
BOOT_7	NAND_IO_7	SDXC_D7_C		
BOOT_8	NAND_IO_CE0			
BOOT_9	NAND_IO_CE1			
BOOT_10	NAND_IO_RB0			
BOOT_11	NAND_ALE	NOR_D		
BOOT_12	NAND_CLE	NOR_Q		
BOOT_13	NAND_WEN_CLK	NOR_C		
BOOT_14	NAND_REN_CLK			
BOOT_15	NAND_DQS			
BOOT_16	NAND_CE2	SDXC_CMD_C	SD_CMD_C	
BOOT_17	NAND_CE3	SDXC_CLK_C	SD_CLK_C	
BOOT_18		NOR_CS		

Table 8. GPIOH_x Multi-Function Pin

Pin Name	Func1	Func2
GPIOH_0	HDMI_HPD	
GPIOH_1	HDMI_SDA	
GPIOH_2	HDMI_SCL	
GPIOH_3	HDMI_CEC	SPI_SS0
GPIOH_4		SPI_MISO
GPIOH_5		SPI_MOSI
GPIOH_6		SPI_SCLK
GPIOH_7	I2C_SDA_D	
GPIOH_8	I2C_SCL_D	
GPIOH_9	CLK_24M_OUT, CLK_12M_OUT	

Table 9. GPIOZ_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOZ_0	I2C_SDA_A	PWM_A		PWM_VS
GPIOZ_1	I2C_SCK_A	PWM_B		PWM_VS
GPIOZ_2	I2C_SDA_B			
GPIOZ_3	I2C_SCK_B			
GPIOZ_4	I2C_SDA_C			
GPIOZ_5	I2C_SCK_C	ETH_TX_EN		
GPIOZ_6		ETH_TXD1		CLK_24M_OUT, CLK_12M_OUT
GPIOZ_7		ETH_TXD0	PWM_VS	PWM_A
GPIOZ_8		ETH_RX_CLK_IN ETH_RX_CLK_OUT	PWM_VS	PWM_C
GPIOZ_9	SPI_SS0	ETH_RX_DV	I2C_SDA_A	
GPIOZ_10	SPI_SS1	ETH_RXD1	I2C_SCK_A	
GPIOZ_11	SPI_SCLK	ETH_RXD0	I2C_SDA_A	
GPIOZ_12	SPI_MOSI	ETH_MDIO	I2C_SCK_A	
GPIOZ_13	SPI_MISO	ETH_MDC		
GPIOZ_14	SPI_SS2			

Table 10. GPIOAO_x Multi-Function Pin

Pin Name	Func1	Func2	Func3
GPIOAO_0	UART_TX_AO_A		UART_TX_AO_B
GPIOAO_1	UART_RX_AO_A		UART_RX_AO_B
GPIOAO_2	UART_CTS_AO_A		
GPIOAO_3	UART_RTS_AO_A		
GPIOAO_4	I2C_MST_SCK_AO	I2C_SLAVE_SCK_AO	UART_TX_AO_B
GPIOAO_5	I2C_MST_SDA_AO	I2C_SLAVE_SDA_AO	UART_RX_AO_B
GPIOAO_6	CLK_32K_IN CLK_32K_OUT		
GPIOAO_7	REMOTE_INPUT		
GPIOAO_8	JTAG_TCK	I2S_AM_CLK	
GPIOAO_9	JTAG_TMS	I2S_AO_CLK	
GPIOAO_10	JTAG_	I2S_LR_CLK	
GPIOAO_11	JTAG_	I2S_OUT_01	
GPIOAO_12	HDMI_CEC		
GPIOAO_13	REMOTE_OUTPUT		
TEST_N	GPIOAO_14 (output only)		PWM_F

Table 11. CSI_x Multi-Function Pin

Pin Name	Func1
CSI_0_p	TSin_D0_B
CSI_0_n	TSin_D1_B
CSI_1_p	TSin_D2_B
CSI_1_n	TSin_D3_B
CSI_2_p	TSin_D4_B
CSI_2_n	TSin_D5_B
CSI_3_p	TSin_D6_B
CSI_3_n	TSin_D7_B
CSI_4_p	TSin_CLK_B
CSI_4_n	TSin_SOP_B
CSI_5_p	TSin_D_VALID_B
CSI_5_n	TSin_FAIL_B

3.5 Signal Descriptions

Table 12. SD Interface Signal Description

Signal Name	Type	Description
SD_D0_A / SDXC_D0_A	DIO	SD/SDXC/SDIO Port A data bus bit 0 signal
SD_D1_A / SDXC_D1_A	DIO	SD/SDXC/SDIO Port A data bus bit 1 signal
SD_D2_A / SDXC_D2_A	DIO	SD/SDXC/SDIO Port A data bus bit 2 signal
SD_D3_A / SDXC_D3_A	DIO	SD/SDXC/SDIO Port A data bus bit 3 signal
SDXC_D4_A	DIO	SDXC/SDIO Port A data bus bit 4 signal
SDXC_D5_A	DIO	SDXC/SDIO Port A data bus bit 5 signal
SDXC_D6_A	DIO	SDXC/SDIO Port A data bus bit 6 signal
SDXC_D7_A	DIO	SDXC/SDIO Port A data bus bit 7 signal
SD_CLK_A / SDXC_CLK_A	DO	SD/SDXC/SDIO Port A clock signal
SD_CMD_A / SDXC_CMD_A	DIO	SD/SDXC/SDIO Port A command signal
SD_D0_B / SDXC_D0_B	DIO	SD/SDXC/SDIO Port B data bus bit 0 signal
SD_D1_B / SDXC_D1_B	DIO	SD/SDXC/SDIO Port B data bus bit 1 signal
SD_D2_B / SDXC_D2_B	DIO	SD/SDXC/SDIO Port B data bus bit 2 signal
SD_D3_B / SDXC_D3_B	DIO	SD/SDXC/SDIO Port B data bus bit 3 signal
SD_CLK_B	DO	SD/SDXC/SDIO Port B clock signal
SD_CMD_B	DIO	SD/SDXC/SDIO Port B command signal
SD_D0_C / SDXC_D0_C	DIO	SD/SDXC/SDIO Port C data bus bit 0 signal
SD_D1_C / SDXC_D1_C	DIO	SD/SDXC/SDIO Port C data bus bit 1 signal
SD_D2_C / SDXC_D2_C	DIO	SD/SDXC/SDIO Port C data bus bit 2 signal
SD_D3_C / SDXC_D3_C	DIO	SD/SDXC/SDIO Port C data bus bit 3 signal
SDXC_D4_C	DIO	SDXC/SDIO Port C data bus bit 4 signal
SDXC_D5_C	DIO	SDXC/SDIO Port C data bus bit 5 signal
SDXC_D6_C	DIO	SDXC/SDIO Port C data bus bit 6 signal
SDXC_D7_C	DIO	SDXC/SDIO Port C data bus bit 7 signal
SD_CLK_C / SDXC_CLK_C	DO	SD/SDXC/SDIO Port C clock signal
SD_CMD_C / SDXC_CMD_C	DIO	SD/SDXC/SDIO Port C command signal

Table 13. Clock Interface Signal Description

Signal Name	Type	Description
XTAL_32K_OUT	DO	32KHz XTAL oscillator output
XTAL_24M_OUT	DO	24MHz XTAL oscillator output
XTAL/2	DO	XTAL/2 oscillator output
CLK_12M_OUT	DO	12MHz XTAL clock output
CLK_32K_OUT	DO	32KHz XTAL clock output
CLK_32K_IN	DI	32KHz XTAL clock input

Table 14. UART Interface Signal Description

Signal Name	Type	Description
UART_TX_A	DO	UART Port A data output
UART_RX_A	DI	UART Port A data input
UART_CTS_A	DI	UART Port A Clear To Send Signal
UART_RTS_A	DO	UART Port A Ready To Send Signal
UART_TX_B	DO	UART Port B data output
UART_RX_B	DI	UART Port B data input
UART_CTS_B	DI	UART Port B Clear To Send Signal
UART_RTS_B	DO	UART Port B Ready To Send Signal
UART_TX_C	DO	UART Port C data output

Signal Name	Type	Description
UART_RX_C	DI	UART Port C data input
UART_CTS_C	DI	UART Port C Clear To Send Signal
UART_RTS_C	DO	UART Port C Ready To Send Signal
UART_TX_AO_A	DO	UART Port AO_A data output
UART_RX_AO_A	DI	UART Port AO_A data input
UART_CTS_AO_A	DI	UART Port AO_A Clear To Send Signal
UART_RTS_AO_A	DO	UART Port AO_A Ready To Send Signal
UART_TX_AO_B	DO	UART Port AO_B data output
UART_RX_AO_B	DI	UART Port AO_B data input
UART_CTS_AO_B	DI	UART Port AO_B Clear To Send Signal
UART_RTS_AO_B	DO	UART Port AO_B Ready To Send Signal

Table 15. PCM Interface Signal Description

Signal Name	Type	Description
PCM_OUT_A	O	PCM port A output data stream
PCM_IN_A	I	PCM port A input data stream
PCM_FS_A	O	PCM port A frame synchronization
PCM_CLK_A	O	PCM port A master clock input
PCM_OUT_B	O	PCM port B output data stream
PCM_IN_B	I	PCM port B input data stream
PCM_FS_B	O	PCM port B frame synchronization
PCM_CLK_B	O	PCM port B master clock input

Table 16. TS Interface Signal Description

Signal Name	Type	Description
TSin_D0_A	DI	TS input port A data bus bit 0 (LSB)
TSin_D1_A	DI	TS input port A data bus bit 1
TSin_D2_A	DI	TS input port A data bus bit 2
TSin_D3_A	DI	TS input port A data bus bit 3
TSin_D4_A	DI	TS input port A data bus bit 4
TSin_D5_A	DI	TS input port A data bus bit 5
TSin_D6_A	DI	TS input port A data bus bit 6
TSin_D7_A	DI	TS input port A data bus bit 7 (MSB)
TSin_CLK_A	DI	TS input port A clock
TSin_SOP_A	DI	TS input port A start of stream signal
TSin_D_VALID_A	DI	TS input port A date valid signal
TSin_FAIL_A	DI	TS input port A data failure signal
TSin_D0_B	DI	TS input port B data bus bit 0 (LSB)
TSin_D1_B	DI	TS input port B data bus bit 1
TSin_D2_B	DI	TS input port B data bus bit 2
TSin_D3_B	DI	TS input port B data bus bit 3
TSin_D4_B	DI	TS input port B data bus bit 4
TSin_D5_B	DI	TS input port B data bus bit 5
TSin_D6_B	DI	TS input port B data bus bit 6
TSin_D7_B	DI	TS input port B data bus bit 7 (MSB)
TSin_CLK_B	DI	TS input port B clock
TSin_SOP_B	DI	TS input port B start of stream signal
TSin_D_VALID_B	DI	TS input port B date valid signal
TSin_FAIL_B	DI	TS input port B data failure signal
TSout_D0	DO	TS output data bus bit 0 (LSB)

Signal Name	Type	Description
TSout_D1	DO	TS output data bus bit 1
TSout_D2	DO	TS output data bus bit 2
TSout_D3	DO	TS output data bus bit 3
TSout_D4	DO	TS output data bus bit 4
TSout_D5	DO	TS output data bus bit 5
TSout_D6	DO	TS output data bus bit 6
TSout_D7	DO	TS output data bus bit 7 (MSB)
TSout_CLK	DO	TS output clock
TSout_SOP	DO	TS output start of stream signal
TSout_D_VALID	DO	TS output date valid signal
TSout_FAIL	DO	TS output data failure signal

Table 17. PWM Interface Signal Description

Signal Name	Type	Description
PWM_A	DO	PWM channel A output signal
PWM_B	DO	PWM channel B output signal
PWM_C	DO	PWM channel C output signal
PWM_D	DO	PWM channel D output signal
PWM_E	DO	PWM channel E output signal
PWM_F	DO	PWM channel F output signal
PWM_VS	DO	PWM VSYNC output signal

Table 18. ISO7816 Interface Signal Description

Signal Name	Type	Description
ISO7816_DET	DI	ISO7816 detect signal
ISO7816_RESET	DO	ISO7816 reset signal
ISO7816_CLK	DO	ISO7816 clock signal
ISO7816_DATA	DIO	ISO7816 serial data signal

Table 19. I2C Interface Signal Description

Signal Name	Type	Description
I2C_SDA_A	DIO	I2C bus port A data input/output, Master or Slave
I2C_SCK_A	DIO	I2C bus port A clock input/output, Master or Slave
I2C_SDA_B	DIO	I2C bus port B data input/output, Master or Slave
I2C_SCK_B	DIO	I2C bus port B clock input/output, Master or Slave
I2C_SDA_C	DIO	I2C bus port C data input/output, Master or Slave
I2C_SCK_C	DIO	I2C bus port C clock input/output, Master or Slave
I2C_SDA_D	DIO	I2C bus port D data input/output, Master or Slave
I2C_SCK_D	DIO	I2C bus port D clock input/output, Master or Slave
I2C_MST_SCK_AO	DO	Always-on I2C master serial clock line
I2C_MST_SDA_AO	DIO	Always-on I2C master serial data line
I2C_SLAVE_SCK_AO	DI	Always-on I2C slave serial clock line
I2C_SLAVE_SDA_AO	DIO	Always-on I2C slave serial data line

Table 20. I2S Interface Signal Description

Signal Name	Type	Description
I2S_OUT_01	DO	I2S Audio Data Output channel 0 and 1
I2S_OUT_23	DO	I2S Audio Data Output channel 2 and 3
I2S_OUT_45	DO	I2S Audio Data Output channel 4 and 5
I2S_OUT_67	DO	I2S Audio Data Output channel 6 and 7

Signal Name	Type	Description
I2S_IN_CH01	DI	I2S Audio Data Input channel 0 and 1
I2S_LR_CLK	DO	I2S Left/Right Clock Out
I2S_AO_CLK	DO	I2S data clock output
I2S_AM_CLK	DO	I2S master clock output

Table 21. SPDIF Interface Signal Description

Signal Name	Type	Description
SPDIF_IN	DI	SPDIF input signal
SPDIF_OUT	DO	SPDIF output signal

Table 22. Digital Video Input Interface Signal Description

Signal Name	Type	Description
DVIN_R0	DI	Digital video input red bit 0 (LSB)
DVIN_R1	DI	Digital video input red bit 1
DVIN_R2	DI	Digital video input red bit 2
DVIN_R3	DI	Digital video input red bit 3
DVIN_R4	DI	Digital video input red bit 4
DVIN_R5	DI	Digital video input red bit 5
DVIN_R6	DI	Digital video input red bit 6
DVIN_R7	DI	Digital video input red bit 7 (MSB)
DVIN_G0	DI	Digital video input green bit 0 (LSB)
DVIN_G1	DI	Digital video input green bit 1
DVIN_G2	DI	Digital video input green bit 2
DVIN_G3	DI	Digital video input green bit 3
DVIN_G4	DI	Digital video input green bit 4
DVIN_G5	DI	Digital video input green bit 5
DVIN_G6	DI	Digital video input green bit 6
DVIN_G7	DI	Digital video input green bit 7 (MSB)
DVIN_B0	DI	Digital video input blue bit 0 (LSB)
DVIN_B1	DI	Digital video input blue bit 1
DVIN_B2	DI	Digital video input blue bit 2
DVIN_B3	DI	Digital video input blue bit 3
DVIN_B4	DI	Digital video input blue bit 4
DVIN_B5	DI	Digital video input blue bit 5
DVIN_B6	DI	Digital video input blue bit 6
DVIN_B7	DI	Digital video input blue bit 7 (MSB)
DVIN_VS	DI	Digital video input vertical sync
DVIN_HS	DI	Digital video input horizontal sync
DVIN_CLK	DI	Digital video input clock
DVIN_DE	DI	Digital video input data enable

Table 23. ENC Interface Signal Description

Signal Name	Type	Description
ENC_0	DIO	Programmable interface signal 0
ENC_1	DIO	Programmable interface signal 1
ENC_2	DIO	Programmable interface signal 2
ENC_3	DIO	Programmable interface signal 3
ENC_4	DIO	Programmable interface signal 4
ENC_5	DIO	Programmable interface signal 5
ENC_6	DIO	Programmable interface signal 6

Signal Name	Type	Description
ENC_7	DIO	Programmable interface signal 7
ENC_8	DIO	Programmable interface signal 8
ENC_9	DIO	Programmable interface signal 9
ENC_10	DIO	Programmable interface signal 10
ENC_11	DIO	Programmable interface signal 11
ENC_12	DIO	Programmable interface signal 12
ENC_13	DIO	Programmable interface signal 13
ENC_14	DIO	Programmable interface signal 14
ENC_15	DIO	Programmable interface signal 15
ENC_16	DIO	Programmable interface signal 16
ENC_17	DIO	Programmable interface signal 17

Table 24. VGA Interface Signal Description

Signal Name	Type	Description
VGA_HS	DO	VGA output horizontal sync signal
VGA_VS	DO	VGA output vertical sync signal

Table 25. NAND Interface Signal Description

Signal Name	Type	Description
NAND_IO_0	DIO	NAND data bus bit 0
NAND_IO_1	DIO	NAND data bus bit 1
NAND_IO_2	DIO	NAND data bus bit 2
NAND_IO_3	DIO	NAND data bus bit 3
NAND_IO_4	DIO	NAND data bus bit 4
NAND_IO_5	DIO	NAND data bus bit 5
NAND_IO_6	DIO	NAND data bus bit 6
NAND_IO_7	DIO	NAND data bus bit 7
NAND_IO_CE0	DO	NAND chip enable 0
NAND_IO_CE1	DO	NAND chip enable 1
NAND_CE2	DO	NAND chip enable 2
NAND_CE3	DO	NAND chip enable 3
NAND_IO_RB0	DI	NAND ready/busy
NAND_ALE	DO	NAND address latch enable:
NAND_CLE	DO	NAND command latch enable:
NAND_WEN_CLK	DO	NAND write enable and clock:
NAND_REN_CLK	DO	NAND read enable and write/read:
NAND_DQS	DIO	NAND data strobe

Table 26. NOR Interface Signal Description

Signal Name	Type	Description
NOR_D	DO	SPI NOR Master Output
NOR_Q	DI	SPI NOR Master Input
NOR_C	DO	SPI NOR Serial Clock
NOR_CS	DO	SPI NOR chip select

Table 27. Boundary Scan Interface Signal Description

Signal Name	Type	Description
GPO_BSD	DO	Boundary scan enable signal
BSD_TDO	DO	Boundary scan data output

Signal Name	Type	Description
BSD_TDI	DI	Boundary scan data input
BSD_TMS	DI	Boundary Test mode select input
BSD_TCK	DI	Boundary Test clock input

Table 28. HDMI Interface Signal Description

Signal Name	Type	Description
HDMI_HPD	DI	HDMI hot plug in detection signal input
HDMI_SDA	DIO	HDMI I2C control interface data signal
HDMI_SCL	DO	HDMI I2C control interface clock signal
HDMI_CEC	DIO	HDMI CEC (Consumer electronics control)

Table 29. SPI Interface Signal Description

Signal Name	Type	Description
SPI_MOSI	DIO	SPI master output, slave input
SPI_MISO	DIO	SPI master input, slave output
SPI_SCLK	DIO	SPI serial clock
SPI_SS0	DIO	SPI slave select 0
SPI_SS1	DIO	SPI slave select 1
SPI_SS2	DIO	SPI slave select 2

Table 30. Ethernet Interface Signal Description

Signal Name	Type	Description
ETH_RX_CLK_IN	DI	Ethernet RMII interface receive clock input
ETH_RX_CLK_OUT	DO	Ethernet RMII interface receive clock output
ETH_RX_DV	DI	Ethernet RMII receive data valid signal
ETH_RXD1	DI	Ethernet RMII interface receive data 1
ETH_RXD0	DI	Ethernet RMII interface receive data 0
ETH_TX_EN	DO	Ethernet RMII interface transmit enable
ETH_TXD1	DO	Ethernet RMII interface transmit data 1
ETH_TXD0	DO	Ethernet RMII interface transmit data 0
ETH_MDC	DO	Ethernet RMII interface management data clock
ETH_MDIO	DIO	Ethernet RMII interface management data input/output

Table 31. Remote Interface Signal Description

Signal Name	Type	Description
REMOTE_INPUT	DI	IR remote control input
REMOTE_OUTPUT	DO	IR remote control output

Table 32. JTAG Interface Signal Description

Signal Name	Type	Description
JTAG_TDO	DO	JTAG data output
JTAG_TDI	DI	JTAG data input
JTAG_TMS	DI	JTAG Test mode select input
JTAG_TCK	DI	JTAG Test clock input

4. Operating Conditions

4.1 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Characteristic	Value	Unit
VDD_CPU Supply Voltage	1.3	V
VDD_EE Supply Voltage	1.3	V
VDDQ Supply Voltage	1.75	V
RTC_VBAT Supply Voltage	1.25	V
1.8V Supply Voltage	1.98	V
3.3V Supply Voltage	3.63	V
Input voltage, V_I	-0.3 ~ VDDIO+0.3	V
Junction Temperature	125	°C

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDCPU	Voltage For Cortex A9 CPU	0.77[1]	0.9	1.19[2]	V
VDDEE_0V9	Voltage For GPU & core logic	0.77[1]	0.9	1.19[2]	V
VDDCORE_AO	Voltage For Always On core logic	0.77[1]	0.9	1.19[2]	V
VDDQ	DDR3/LPDDR2/LPDDR3 IO Supply Voltage	1.15		1.6	V
AVDD18	1.8V AVDD for Audio codec, CSI, CVBS, HDMI, PLL, SARADC, USB, XTAL, EFUSE_VDD1V8, IOVREF_1V8	1.71	1.80	1.89	V
USB_VDD33	3.3V AVDD for USB	3.15	3.3	3.45	V
VDDIO	LV mode	1.71	1.80	1.89	V
	HV mode[3]	2.8	3.3	3.45	V
RTC_VBAT	Supply voltage for RTC	0.7	0.90	1.1	V
T_J	Junction Temperature	0		125[4]	°C
T_A	Operating Temperature	0		70	°C

Note:

1) Minimal VDD_CPU/VDD_EE voltage is for sleep mode while system runs at 32KHz. Higher clock will need higher voltage. Considering the power supply may have 3% deviation, the minimal voltage in actual application should not be set to lower than 0.8V.
2) Likewise, this maximum VDD_CPU/VDD_EE voltage in actual application should not be higher than 1.15V. Voltage of VDD_CPU will affect CPU speed. Use lower voltage when CPU runs on lower speed to save power.
3) GPIO output driving strength will be weaker when VDDIO < 3.0V in HV mode. Signal ramp-up speed & max operation speed are lower than VDDIO at 3.3V.
4) For operating temperature, good heat sink may be needed to guarantee Tj < 125°C.

4.3 Thermal Operating Specifications

Symbol	Parameter	Value.	Unit
Θjc	Package junction-to-case thermal resistance in nature convection	4.14	°C/Watt

4.4 DDR3/LPDDR2/LPDDR3 SDRAM Specifications

4.4.1 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDQ	IO supply voltage(DDR3)	1.46	1.50	1.57	V
VDDQ	IO supply voltage(DDR3L)	1.31	1.35	1.45	V
VDDQ	IO supply voltage(DDR3U)	1.21	1.25	1.31	V
VDDQ	IO supply voltage(LPDDR2/LPDDR3)	1.16	1.20	1.30	V
Vref	Input reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V

Note: The minimal VDDQ voltage in sleep mode is defined by memory.

4.4.2 DC specifications - DDR3/DDR3L/DDR3U mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.8*VDDQ			V
VOL	DC output logic low			0.2*VDDQ	V
RTT	Input termination resistance to VDDQ/2	100 54 36	120 60 40	140 66 44	ohm

4.4.3 DC Specifications – LPDDR2 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.13		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.13	V
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V

4.4.4 DC Specifications – LPDDR3 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	100 200	120 240	140 280	ohm

4.5 Recommended Oscillator Electrical Characteristics

S802 requires two oscillators for input clocks. The 32.768KHz oscillator is used for low frequency operations.

Table 33. 32.768KHz Oscillator Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_o	Nominal Frequency		32.768		KHz	
$\Delta f/f_o$	Frequency Tolerance	-30		+30*	ppm	At 25 ℃
		-150		+150	ppm	At -20~85 ℃

Note: 10ppm Tolerance is preferred to get accurate RTC time.

And the 24MHz oscillator is applied for generating the main clock source.

Table 34. 24MHz Oscillator Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_o	Nominal Frequency		24		MHz	
$\Delta f/f_o$	Frequency Tolerance	-30		+30	ppm	At 25 ℃
		-50		+50	ppm	At -20~85 ℃

Note: 10ppm Tolerance is preferred if 24MHz XTAL is also driving WIFI module.

4.6 Recommended Power on sequence

Example power on sequence：

* VDDEE_0V9 & VDDCPU -> IOVREF_1V8 -> VDDIO_AO18 -> VDDIO_AO28 -> VDDIO3.3V -> VDDQ -> VDDIO1.8V & AVDD1.8V

Note:

* Limit the power source current of VDDEE_0V9 & VDDCPU to 0.5A when system power on or wakeup (> 18ms)

1) No sequence demand between power domains which are put in one slot in example sequence.
2) VDDQ can be off and enabled by software.
3) Step delay should be 0-4ms. (IOVREF_1V8 -> VDDIO_AO18 must be delayed at least 15ms.)
4) VDDIO_AO18 & VDDIO1.8V must be held low (<0.1V) before power up.
5) VDDIO3.3V should never exceed IOVREF_1V8 + 2V.
6) Reset should be kept low before power up & kept low > 40ms after all power is on (except VDDQ)
7) VDDIO_AO18 is for some GPIOs such as WiFi IO.
   VDDIO_AO28 is for GPIOAO & some GPIOs such as 2G/3G IO.

Please refer to reference schematics.

4.7 Power consumption

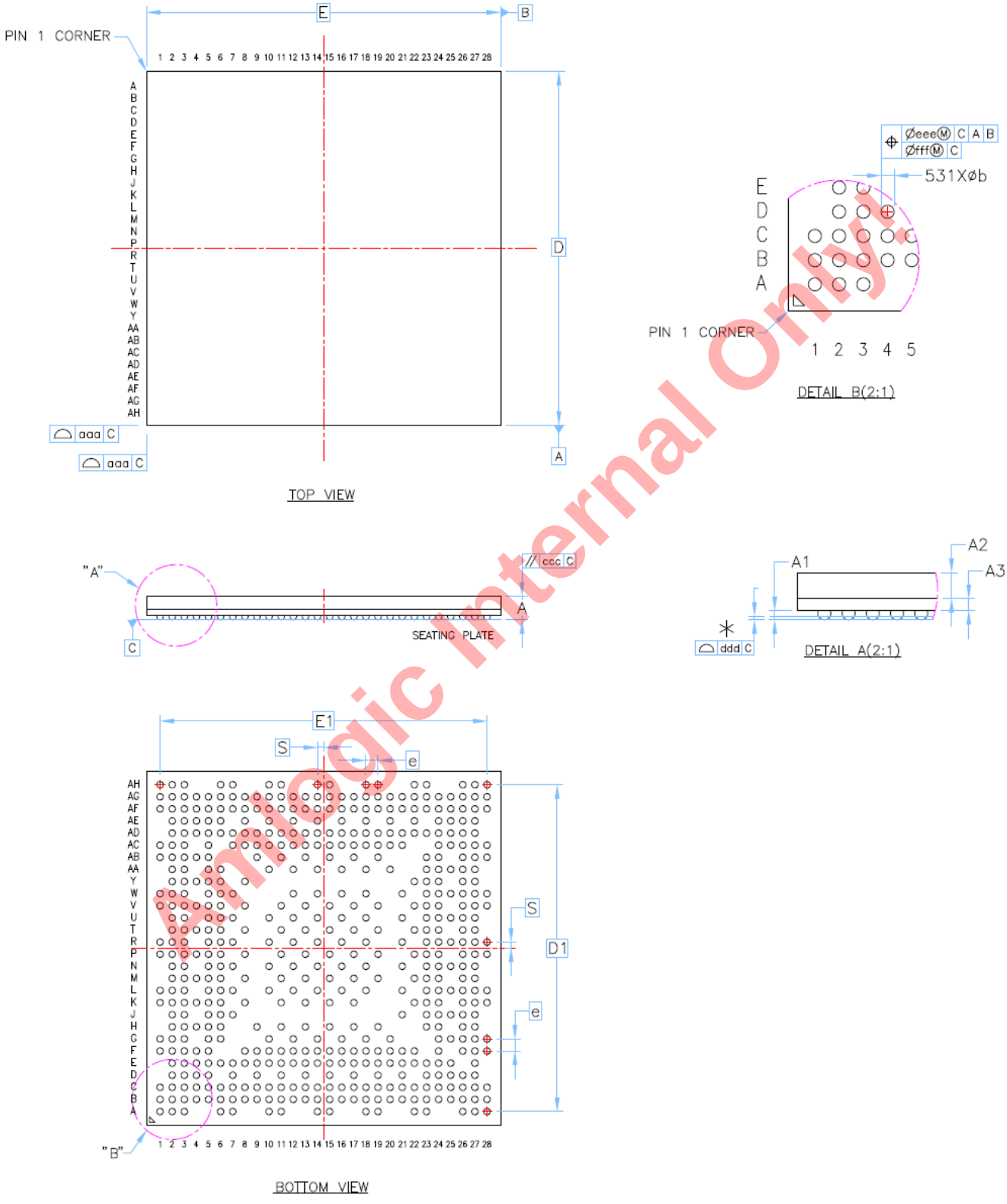
Note：Value listed here is typical max value tested. Enough margin in circuit needs to be reserved.

Symbol	Maximum Current	Note
VDDCPU	2000mA	
VDDEE_0V9	2000mA	
VDDQ	1000mA	Total power of controller and DDR3 memory

Symbol	Typical current	Note
USB_VDD18	19mA	Per channel, high speed mode , total 2 channel
USB_VDD33	16mA	Per channel, full/low speed mode, total 2 channel
CSI_AVDD18	TBD	
HDMI_AVDD18 HDMITX_AVDD18	TBD	
CVBS_AVDD18	40mA	
AVDD18_HPLL	8mA	
VDDIO_XTAL_18	0.4mA	
PLL_VDD	32mA	Per DDR3 channel
IOVREF_1V8	20mA	Max 20mA when all GPIO powered with 3.3V & switch at 75MHz. Normally 0mA.
EFUSE_VDD1V8,	100mA	Max 100mA when programing EFUSE. Normally 0mA.
RTC_VBAT	4uA	3~10uA @ 0.9V

5. Mechanical Dimensions

The S802 processor comes in a 531 balls LFBGA RoHS package. The mechanical dimensions are given in millimeters as below:



FOR CUSTOMER ONLY				
PACKAGE TYPE	LFBGA			
PIN COUNT	531			
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	–	1.27	1.37
STAND OFF	A1	0.20	0.25	0.30
MOLD THICKNESS	A2	–	0.70 BSC	–
MATERIAL THICKNESS	A3	0.28	0.32	0.36
PACKAGE SIZE	D	18.90	19.00	19.10
	E	18.90	19.00	19.10
BALL PITCH	e		0.65 BSC	
BALL SIZE	b	0.30	0.35	0.40
EDGE BALL CENTER TO CENTER	D1	–	17.55 BSC	–
	E1	–	17.55 BSC	–
PACKAGE EDGE PROFILE	aaa		0.10	
SUBSTRATE FLATNESS	bbb		–	
MOLD FLATNESS	ccc		0.10	
BALL COPLANARITY	ddd		0.10	
BALL POSITION OFFSET (PACKAGE)	eee		0.15	
BALL POSITION OFFSET (BALL)	fff		0.08	
	S		0.325	